Master Thesis Proposal

Efficient Analog Modelling of Multi-Input Gates

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1 Problem Statement

Simulating digital circuits is an important task and should be conducted as early as possible in the design process. Contemporary tools mainly use two approaches of simulating such circuits: On the one hand analog simulators yield highly accurate results but are slow, on the other hand digital simulators are fast, but hide a lot of details. An approach that combines the advantages of both methods would be desirable. This approach should especially work for complex gates and cover the respective effects governing such gates, in particular the so called Charlie effect [1].

2 Expected Result

The aim of this thesis is to develop a tool using a new simulation approach. This approach treats analog signals as lists of transitions that are characterized by a small set of parameters. From these parameters, i.e., buy summing up the respective transitions, the analog signal traces can be calculated. Upon propagation through the circuits the transition parameters are supposed to be changed according to the changes the analog signals experience. The target of the analyses in this thesis will be a two-input gate, more specifically a NOR-Gate.

At first a large number of SPICE [2] simulations shall be executed to establish a relationship between input and output parameters. Using this relationship, the propagation of a transition through a NOR-Gate can be simulated with very low computational effort. One of the main concerns, however, is modelling the Charlie effect [1]. This effect causes output transitions to speed up or slow down (depending on the transition polarity) if the time difference between the input transitions of both inputs is small.

In the end, the following questions shall be answered: Can the tool accurately model the Charlie effect? How accurate are the simulations in comparison to SPICE? What is the speed difference between the tool and SPICE/commercial digital tools?

3 Methods

- Literature Review
  - Information will be gathered about existing approaches for modelling multi-input gates.
- Simulation
  - A variety of circuits has to be systematically simulated in SPICE to gather data for the succeeding step.
- Modelling
  - Based on the retrieved data, a model will be generated that allows an accurate description of the analog behaviour at very limited computational effort.
- Analysis
  - The built model is compared to SPICE simulations and the commercial digital timing tool QuestaSim.
- Evaluation
  - Research questions, especially concerning the accuracy and performance compared to other simulation approaches, will be answered.

Several iterations of the steps Simulation, Modelling and Analysis will be applied until no further progress in model accuracy is achievable.

4 State of the Art

Contemporary tools like SPICE [2], use highly sophisticated analog models like BSIM [3] to simulate circuits. SPICE yields accurate results while consuming a lot of time and computational effort. In this thesis it is considered the golden standard against which any other simulation method must be measured in terms of simulation accuracy.

On the other hand digital simulators enhanced with characteristic delay behaviours operate on high abstraction levels. The delay of a cell is estimated from SPICE simulations across varying input slopes and output loads [4]. The tabulated results are used to parameterize pure or inertial delay channels [5, 6]. The pure delay channel simply adds a constant delay to a transition propagating a cell. In addition to that, the inertial delay channel also removes transitions that are too close to each other. This approach uses less resources but approximates signals by zero time transitions, providing no information about the shape of the signal. Although the run time effort is considerably lower than SPICE, the characterisation effort should not be underestimated.

Alternative methods situated in between these two established approaches have already been proposed in literature. One approach is to perform a series-parallel reduction of the transistors in a gate and treat it as an inverter [7]. Another approach called MCSM (multi-port current source model) [8] refines current source models to accurately handle multiple ports at the same time.

In this thesis we aim to improve accuracy with negligible additional effort. Based on the tool developed in [9].

The approach developed in this thesis is situated in-between these two established approaches. In particular a small amount of resources should be used, while providing a reasonable amount of information about the shape of the signal. Similar to the second approach a significant amount of characterisation effort has to be conducted.

5 Relevance to the Master programme Computer Engineering

This thesis aims to improve the efficiency of simulating digital circuits and is therefore relevant to courses concerned with developing such circuits. These courses include:

- 182.754 & 182.755 Advanced Digital Design
- 182.700 & 182.701 HW/SW Codesign

References

[1] J.C. Ebergen, S. Fairbanks, and I.E. Sutherland. Predicting performance of micropipelines using charlie diagrams. In *Proceedings Fourth International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 238–246, 1998.

[2] Laurence Nagel and Donald O Pederson. Spice (simulation program with integrated circuit emphasis). 1973.

[3] B. J. Sheu, D. L. Scharfetter, P. . Ko, and M. . Jeng. Bsim: Berkeley short-channel igfet model for mos transistors. *IEEE Journal of Solid-State Circuits*, 22(4):558–566, Aug 1987.

[4] CCS Timing Library Characterization Guidelines. *Synopsis Inc.*, October 2016, version 3.4.

[5] S. H. Unger. *Asynchronous sequential switching circuits*. Wiley-Interscience, 1969.

[6] M. J. Bellido-Diaz, J. Juan-Chico, A. J. Acosta, M. Valencia, and J. L. Huertas. Logical modelling of delay degradation effect in static cmos gates. *IEE Proceedings - Circuits, Devices and Systems*, 147(2):107–117, April 2000.

[7] Young-Hyun Jun, Ki Jun, and Song-Bai Park. An accurate and efficient delay time modeling for mos logic circuits using polynomial approximation. *IEEE transactions on computer-aided design of integrated circuits and systems*, 8(9):1027–1032, 1989.

[8] C. Amin, C. Kashyap, N. Menezes, K. Killpack, and E. Chiprout. A multiport current source model for multiple-input switching effects in cmos library cells. In *2006 43rd ACM/IEEE Design Automation Conference*, pages 247–252, 2006.

[9] Josef Salzmann. Approximating analog waveforms by adding arbitrary functions. B.S. Thesis, TU Wien, 2021.