Masterthesis proposal

η-CIDM: A faithful and composible delay model with adversarial noise

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1 Context and Overview

Predicting the delay of signals through a digital circuit is an important task in digital design. While analog simulations, e.g. SPICE, are very accurate, their simulation times are excessive. On the other hand, most digital delay models lack faithfulness, which is an important property, especially when it comes to formal verification of digital circuits.

To the best of our knowledge, the only known candidate for a faithful delay model is the Involution Delay Model (IDM) [FNNS20], as its faithfulness has been proved for the Short-Pulse Filtration (SPF) problem: The unbounded version of the SPF problem can be solved in physical reality, whereas its bounded counterpart cannot be solved. By showing that IDM behaves exactly like physical reality, the faithfulness of this delay model follows.

Several extensions of the IDM exist, most notably the Composable IDM (CIDM) [MÖS$^+$] and η-IDM [FMN$^+$18]. The first extension aims at simplifying gate characterization, by allowing to combine gates with different threshold voltages. The second extension allows adding delay variations to extend the modelling power. These delay variations, which can be random or adversarial, are added on top of the actual delay calculation but have to be in a relatively narrow range between $[\eta^-, \eta^+]$.

The goal of this thesis is to combine both extensions into a faithful delay model η-CIDM, which allows adversarial or random delay variations, but still maintains the easy composability of CIDM. We will address the following three challenges:

(1) We will show the possibility of unbounded SPF and the impossibility of bounded SPF in η-CIDM. One viable approach for achieving this is to use reductions.

(2) One of the strengths of delay models that allow delay variations is their superior ability to model process variations and aging effects. On the other hand, CIDM is especially useful when the threshold voltage between gates varies, which is unavoidable in a real circuit. Therefore, we are going to examine η-CIDM for its applicability in such scenarios by extensive simulations.

(3) Currently, η-IDM has strict constraints $[\eta^-, \eta^+]$ on the delay variations. These constraints seem to be required for short pulses only, so we will investigate if it is possible to loosen them for broader pulses.

2 Expected Results

We will create a new extension η-CIDM of IDM which should allow to accurately model the behaviour of circuits which are subject to process, voltage and temperature variations (PVT variations), aging, and threshold variations.

3 Methodological Approach

The expected results shall be achieved in three reasonably orthogonal steps, which can in part be performed concurrently.

3.1 Proving faithfulness of the new extension

In this step, the goal is to show that the new extension, which combines composability and delay variations, is still faithful. We plan to do this with a reduction from η-CIDM to η-IDM. The structure of the reduction is similar to the one of [MÖS$^+$, Theorem 8, Theorem 10].

3.2 Simulations

In the next step, we perform extensive simulations to compare our new digital delay model with the golden reference SPICE. For the digital simulations, we employ the Involution Tool [ÖMFS21], a framework where CIDM has already been implemented. The goal is to run the SPICE simulations under different PVT variations and check if the estimated delays are within the range of delay variations allowed by η-CIDM. Moreover, we will us aging SPICE libraries to examine if the delay predictions are still accurate when considering aging circuits. As a starting point for these simulations, publicly available degradation-aware cell libraries [AKGH16] are used.

3.3 Loosening constraints for the delay variations

In the final step, we investigate the constraints on η^+ and η^-, which are currently necessary in η-IDM. Especially for larger pulse widths, we assume that these constraints can be loosened.

Moreover, the current reduction proof for the impossibility of bounded SPF in η-IDM always chooses the delay variation $\eta_n = 0$. Therefore, this case directly degenerates to IDM. Since CIDM is able to cope with different threshold voltages by using variable pure delays, it would be interesting to find a reduction proof for a deterministic adversary which delays rising and falling transitions by a fixed value $\eta^\uparrow \neq 0$ and $\eta^\downarrow \neq 0$. A deterministic delay of rising and falling transition models variations in threshold voltages, and is therefore of interest in terms of composability.

4 State of the Art

4.1 Delay models

Pure and inertial delay model [Ung71] are simple delay models where each input transition is delayed by a constant δ. In case of the inertial delay model, input pulses with a width $\leq \Delta$ are rejected. Függer et al. [FNS16] proved that these

delay models are unfaithful. Nevertheless, they are widely used, for example in VHDL Vital [IEE01, Chapter 9] or the Verilog delay model [IEE06, Chapter 14].

The actual delay values which are used to parametrize the pure and inertial delay model are obtained for example with CCSM [Syn16] and ECSM [Cad15]. These methods measure the delay for different input slews and load capacitances, which results in a table containing the results for different delays. The delays for each cell are than picked from the table. However, once the delay has been picked, it remains constant throughout all simulations.

One of the problems of inertial delay is its discontinuity. Pulses with a width $\leq \Delta$ are rejected, whereas a pulse with width $\Delta + \varepsilon$ ($\varepsilon > 0$) is passed unaltered. A delay model which tackles this issue is the Degradation Delay Model (DDM) [BDJCA$^+$00]. It introduces the degradation region, where depending on the time since the last output transition T the pulses are degraded until they are finally cancelled if T gets too small. However, Függer et al. [FNS16] proved that this delay model solves bounded SPF, which contradicts the physical reality, and it is therefore also unfaithful.

4.2 Involution delay model (IDM)

The Involution Delay Model has been introduced by Függer et al. [FNNS20] and it is the only known faithful delay model. The delay is calculated based on the previous-output-to-input delay T. Unlike all existing other delay models, the delay functions are unbounded from below. One of its key features is that its negative delay functions form involutions.

η-IDM [FMN$^+$18] is an extension, which allows to add delay variations, making the delay model more applicable. In order to reduce the gate characterization effort, the CIDM has been proposed in [MÖS$^+$]. It allows to combine gates with different threshold voltages by introducing variable pure delays, which compensate for differences between two connected gates.

5 Relation to Computer Engineering

Working at the intersection of hardware and software, and the combination between theoretical foundation and practical experiments, are two key points in the Computer Engineering curricula. The topics of this thesis are a combination of these.

Digital timing models play a vital role during the design and sign-off of digital circuits. Developing and improving such delay models is especially related to the key area *Digital Circuits and Systems*. The necessary skills for obtaining the proofs are taught in *Discrete Mathematics* and *Formal Methods in Computer Science*. The formal verification aspect of this thesis is covered by the key area *Computer-Aided Verification*.

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