Master Thesis Proposal

Smart SoC-Testing facilitated by the usage of IJTAG complemented with onboard microprocessor access

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1 Problem Statement

Designing digital integrated circuits (ICs) requires a high amount of validation and verification throughout the entire process. However, even when implementing a properly verified design in silicon, minor imperfections can lead to defects in the final dies. For this reason, extensive end-of-line (EOL) testing is employed to ensure functionality of the individual device. A widespread concept for design for testing (DFT) is the use of scan chains in the design which allow to control and observe internal logic function via flip-flops.

Modern system on chips (SoCs) contain an ever increasing number of embedded elements. This includes analog and mixed-signal peripherals which cannot be connected to the system bus, yet require runtime configuration via the central processing unit (CPU). The high variety of different configurations within a product family causes further growth in effort and time required for EOL testing and, in turn, results in higher cost and time to market. Moreover, the classical and generally accepted approach of testing established by the JTAG standard is relatively rigid and becoming increasingly unwieldy. On the other hand, the typical testing processes are designed and optimized for the use of JTAG and benefit from widespread tool support.

In addition to EOL testing, built in self tests (BISTs) are becoming increasingly important for complex systems to ensure proper functionality in-field. While the concept is in principle orthogonal to EOL testing, it allows for reuse of hardware required for both practices and can even alleviate testers during EOL testing.

It is therefore of interest to develop a testing solution which is compliant with existing test infrastructure but also offers capabilities for flexible and smart CPU-based testing as well as reuse of scan chains during the productive lifespan of SoCs.

2 Expected Results

The aim of this thesis is the development and implementation of on-chip testing infrastructure based on the recent IJTAG standard for a RISC-V SoC. In particular, the concept shall support transparent operation via a JTAG TAP-controller for conventional EOL testing, as well as via the CPU for the purpose of software-based smart testing. Moreover, reuse of scan chains shall enable configuration of peripherals which cannot be connected to the system bus. At the end of the thesis,

the following questions shall be answered: How can scan chains be reused by the CPU for the purpose of runtime testing and configuration? What reduction in time spent on external testing infrastructure can be expected from CPU-based smart testing? In what way can the solution be designed to ensure extensibility and configurability with respect to future additions and product variety?

3 Methods

For the most part, work on the thesis can be split into multiple phases which may or my not be strictly separated.

3.1 Literature Review

A comprehensive collection of existing literature helps to strengthen theoretical understanding of the topic and forms a strong foundation for the concept and design phase. Besides examination of state of the art approaches, a firm understanding of the JTAG and IJTAG standards are a key requirement.

3.2 Toolchain Knowledge

Infineon has developed a Python-based metamodeling and RTL generation framework called MetaRTL which supports the development of flexible and configurable RTL code generators. The intent is to use this framework for generation of the proposed design. Therefore, solid knowledge of MetaRTL is an important prerequisit for the practical design phase. Moreover, it may prove beneficial to obtain an overview of current EDA tool functionality.

3.3 Concept and Design

The aim of this phase is the development of a concept for on-chip testing infrastructure as well as implementation of MetaRTL based generators to realize said solution in hardware. To this end, the acquired knowledge about the JTAG and IJTAG standards shall help to define conforming subsets and extensions to solve the tasks at hand. This information can then be used to define the required metamodels and implement respective hardware generators. An extension of an existing firmware generation tool (Metafirm) may also turn out to be of value with respect to CPU-operation of scan chains.

3.4 Evaluation

After the practical design phase, feasibility of the implementation for the purpose of smart testing and configuration can be analyzed more in-depth and compared to the state of the art. On the basis of the final design, the relevant research questions can be evaluated and, if deemed necessary, further adjustments can be undertaken.

4 State of the Art

Ever since its first introduction in 1990, the IEEE 1149.1 standard [1], commonly called JTAG, has found widespread use for testing of ICs via scan chains. However, with respect to complex modern designs, there are several shortcomings including the rigid and inefficient chaining of test data

registers (TDRs) to form static scan chains and the fact that test vectors are often not portable between different devices. These problems are addressed by the recent IEEE 1687 standard [2] which is often called IJTAG. It extends the ideas of JTAG with a flexible and configurable network of TDRs, as wells as a set of description languages called ICL (instrument connectivity language) and PDL (procedural description language) which enable retargeting of test vectors.

Another major concern is the partitioning of tests in terms of on-chip and off-chip testing [3]. The use of built-in self tests (BISTs) has potential to reduce cost and time spent for EOL testing and allows for execution of test procedures in the field. While the use of service processor connected to a special TAP-controller as described in [7] may be justifiable for larger systems, the implied overhead is in general not feasible for SoCs. For this reason, CPU-based access to JTAG scan chains is considered more practical. Tools like Tessent MissionMode [8] have offered solutions for the design and integration of memory- and CPU-based BISTs for many years. In this case, either data from on-chip memory or the CPU can be used to directly drive the TAP-controller. A similar approach for memory-based health monitoring is chosen by [4] to reduce dependency on an external controller.

In recent years, standardized protocols such as I^2C [10] and UART [6] have been investigated as alternatives to the proven JTAG TAP controller for the purpose of accessing IJTAG networks. The findings are expected to result in the currently work-in-progress IEEE P1687.1 standard [5]. While this may primarily result in further options for interfaces to the test logic, like in [9] which makes use of I^2C for the purpose of digital trimming of analog circuits, it may also result in interesting developments regarding CPU accessbility. Since June 2021, Tessent MissionMode also offers the possibility to generate an APB-operated test controller.

The solution developed over the course of this thesis will have to fulfill aspects of several of the cited sources. On the one hand, the JTAG TAP-controller is a key requirement for off-chip testing and potential future functionality (e.g. debugger). On the other hand, the IJTAG network will also have to be exposed to the CPU via a separate controller for the purpose of on-chip testing and in-field configuration. Moreover, for the sake of productivity, it is beneficial to augment the approach with the possibility of firmware generation.

5 Context

The main concern of the thesis is to implement a metamodel-based framework for the generation of JTAG- and CPU-operable IJTAG infrastructure and related firmware for the purpose of enabling smart testing and runtime hardware configuration. Therefore, it touches upon the topics of digital design, hardware generation, hardware/software codesign, post-silicon verification and computer architecture in general. The most relevant courses of the "Computer Engineering" curriculum include:

- 182.754 Advanced Digital Design LU
- 182.755 Advanced Digital Design VU
- 182.700 HW/SW Codesign VU
- 182.701 HW/SW Codesign LU
- 191.105 Advanced Computer Architecture VU

References

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[10] Hans-Martin von Staudt, Bradford Van Treuren, Jeff Rearick, Michele Portolan, and Martin Keim. Exploring and comparing IEEE P1687.1 and IEEE 1687 modeling of non-tap interfaces. In *2021 IEEE European Test Symposium (ETS)*, pages 1–10, 2021.