Master Thesis Proposal

Quantitative Comparison of the Sensitivity of Delay-Insensitive Design Templates to Transient Faults

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February 2021

Motivation & Problem Statement

Advances in semiconductor technology bring a lot of new challenges. With deep-submicron transistor sizes the timing variations due to process variations are getting worse. Additionally the overall reduction in supply voltages make them more prone to interferences, and they influence the internal timing as well. This is a big problem for synchronous designs, whose clock is based on the worst case time estimation. Therefore the motivation emerges to use asynchronous designs, where the timing is based on matched delays and thus becomes much more robust against this kind of variations [1].

But on the other hand due to the same reasons (deep-submicron transistor sizes and lower supply voltages) the transistors are also more receptive to transient faults. Furthermore asynchronous designs rely on transitions on handshaking signals to work properly. Therefore compared to synchronous designs, asynchronous designs are much more receptive to transient faults. There is a lot of literature about how to harden asynchronous designs, but in general it is a challenging task. So far there doesn't exist a satisfying quantitative comparison of all the different asynchronous design styles with regard to robustness against transient faults [2].

Growing demand of faster systems and increasingly unpredictable process variations will be a big motivation for the industry to switch to asynchronous designs and thus it is necessary to get a better understanding of the impact of transient faults there.

Overall aim

In this thesis we will make a quantitative comparison of the different asynchronous design styles with respect to their robustness against transient faults. To reduce the scope of this thesis we will only consider static 4-phase dual-rail quasi-delay-insensitive (QDI) pipeline styles. [3]

In the first step we will identify interesting candidate styles. Therefore a state of the art study will be conducted. A special focus will be the potential of the robustness against transient faults and the frequency of mentions in literature and usage in real world applications.

With these candidate styles a test matrix for fault injection experiments in a digital circuit simulation will be developed. The test matrix should have the following dimensions:

- Targets Circuit (IIR, Multiplier, Adder ...)
- Structure (linear, back-coupled ...)
- Pipeline Style / Latch (WCHB, Dual CD ...)
- Logic Style (DIMS, Threshold gates ...)
- Data width (8, 16 ...)
- Fill level (bubble-limited/token-limited)
- Delay variations

To not go beyond the scope of a master thesis only promising aspects of the test matrix will be examined.

As a starting point for the simulations a fault injection tool and a synthesis tool for asynchronous designs is already provided. Both tools are functional and there are some preliminary results present. The functionality of these tools will be extended to handle the large scope of needed simulations.

In the last step the simulation result will be evaluated. There the focus will be to make condensed statements of the different properties of the target styles.

Methodological Approach

The methodological approach consists of the following steps:

1. Literature Review
   We will conduct a literature review to get all information about the currently existing various styles and their applications.

2. Target selection
   We will select target styles based on their resilience against transient faults and their popularity.

3. Smart extensive simulations
   We will create a test matrix with all affecting parameters. All possible axes will be evaluated but only promising targets should be simulated extensively to not go beyond the scope of this thesis. Furthermore the simulation experiments will be parallelized and automated as much as possible.

4. Interpretation of the results
   Based on the results we will compare the target styles based on the resilience against transient faults.

Structure of the Work

1. Introduction
2. Related Concepts
3. State of the Art
4. Research question and contribution
5. Comparison and target selection
6. Tooling and simulation
7. Tests and results
8. Conclusion

State-of-the-Art

The concept of asynchronous pipelines has proven itself for more than 30 years [4]. There are a lot of examples showing the feasibility and the advantages of these concepts over synchronous designs. Especially QDI pipelines with dual-rail data channels and 4-phase look most practical [5].

There are a lot of different approaches how to implement QDI designs [5]. And there are also a lot of different methods to make these designs more robust against transient faults [6][7]. In these papers there normally are some results and comparisons to reference implementations, but in general there is a lack of a extensive comparison between them.

Relevance to the Curricula of Computer Engineering

Digital designs and their simulations are an integral part of the curriculum of the bachelor and master study "Computer Engineering". The combination of theoretical analyses and practical execution is a great possibility to deepen the knowledge in the field. The curriculum of "Computer Engineering" touches the topic of this thesis in many aspects. The most directly linked courses are listed in the following:

- 182.707 Advanced Digital Design
- 182.695 Digital Design and Computer Architecture
- 182.047 Digital Design
- 182.081 Electrical Engineering for Computer Engineering

References

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[5] Ozdag, Recep O., and Peter A. Beerel. "High-speed QDI asynchronous pipelines." Proceedings Eighth International Symposium on Asynchronous Circuits and Systems. IEEE, 2002.

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