MCVU – Control Register Summary v1.00

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Version	Date	Remark
1.0	May 19, 2015	Initial release

General Remarks

This document provides a guideline regarding the registers of the ATmega1280 that are checked during the second and the make-up exam.

1 Register Summary

We provide a summary of the most important registers, and the effect of their relevant control-bits. Please note that only the most relevant bits/registers of modules of the ATmega1280 are described here, those which most likely appear at the tests.

Attention: If a control-bit is not listed here, but its register is, then you must not touch it at the test!

1.1 External Interrupts

Make sure you only change the control-bits of the corresponding interrupt!

Register	Bit	Description	Datasheet page
EICRA, EICRB	ISCn0 ISCn1	Controls the activating level	113 ff.
EIMSK	INTn	Enables the interrupt	115

1.2 8-bit Timer/Counter 0

You may have to set the `TCNT0`, `OCR0A`, or `OCR0B` registers. If so, the values of these registers are checked for their correct value at the test!

Register	Bit	Description	Datasheet page
TCCR0A	WGM00, WGM01	Controls the mode of the timer; see datasheet for information on the modes	131
TCCR0B	WGM02		
	CS01, CS02, CS03	Controls the clock source and the prescaler	133
TIMSK0	TOIE0	Enables the Timer Overflow interrupt	134
	OCIE0A, OCIE0B	Enables the Output Compare Math interrupt	134

1.3 16-bit Timer/Counter 1,3,4,5

Make sure you only change the control-bits of the specified timer!
You may have to set the `TCNTn`, `OCRnA`, `OCRnB` or `ICRn` registers. If so, the values of these registers are checked for their correct value at the test!

Register	Bit	Description	Datasheet page
TCCRnA	WGMn0, WGMn1	Controls the mode of the timer; see datasheet p. 148 for information on the modes	158 ff.
TCCRnB	WGMn2, WGMn3		
	CSn1, CSn2, CSn3	Controls the clock source and the prescaler	160 ff.
TIMSKn	TOIEn	Enables the Timer Overflow interrupt	166
	OCIEnA, OCIEnB, OCIEnC	Enables the Output Compare Math interrupt	166
	ICIEn	Enables the Input Capture interrupt	166

1.4 SPI

Register	Bit	Description	Datasheet page
SPCR	SPIE	Enables the interrupt	202
	SPE	Enables the SPI	
	DORD	Controls the data order	
	MSTR	Master/slave select	
	CPOL	Controls the cock polarity	
	CPHA	Controls the clock phase	
	SPR0, SPR1	Selects the clock rate	202 ff.
SPSR	SPI2X		

1.5 UART

You might also have to set the `UBRR` register. If so, the values of this register is checked for its correct value at the test!

Register	Bit	Description	Datasheet page
UCSRnA	U2Xn	Double speed	223 ff.
	MPCMn	Enables the multiprocessor mode	
UCSRnB	RXCIEn	Enables the RX Complete interrupt	224 ff.
	TXCIEn	Enables the TX Complete interrupt	
	UDRIEn	Enables the Data Register Empty interrupt	
	RXENn	Enables the receiver	
	TXENn	Enables the transmitter	
	UCSZn2	Controls the character size; see datasheet p. 226 for details	225 ff.
UCSRnC	UCSZn1, UCSZn0		
	UMSELn1, UMSELn0	Controls the mode of the UART	225 ff.
	UPMn1, UPMn0	Controls the parity	
	USBSn	Controls the number of stop bits	
	UCPOLn	Controls the clock polarity	

1.6 ADC

Register	Bit	Description	Datasheet page
ADMUX	REFS1, REFS0	Selects the reference voltage	289 ff.
	ADLAR	Enables the left adjustment	
	MUX4:0	Selects the analog channel; See datasheet p. 290 ff. for details	
ADCSRB	MUX5		
ADCSRA	ADEN	Enables the ADC	292 ff.
	ADSC	Starts a conversion	
	ADATE	Enables the auto trigger	
	ADIE	Enables the interrupt	
	ADPS2:0	Selects the prescaler; The resulting frequency has to be in the range [50kHz, 200kHz]! See datasheet p. 278 for details	
ADCSRB	ADTS2:0	Controls the source for the auto trigger	294 ff.