VO Hardware Modeling
182.696

Overview Exam Content

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- hardware vs. software implementations
- design languages
- **architecture**, **entity** and **configuration**
- concurrent vs. sequential vs. structural design style: transform code from one to another
- writing a testbench
- low vs. high active, synchronous vs. asynchronous
- memory elements and other basic units
- delays and **wait**
- execution of **process** during simulation
- temporal evolution of signals and variables
- sensitivity list and its effects
- **variable** vs. **signal**
- text $\leftrightarrow$ output and state transition table $\leftrightarrow$ state transition graph $\leftrightarrow$ VHDL code
- two and three process method
- analyze given VHDL code and modify it
- data types: computations, subtypes, vectors and attributes

- real world input problems
- interpret and apply syntax specification like in the VHDL standard
- hardware modeling overview
- hardware design vs. implementation
- the almighty clock
- code reusability
- timing analysis
- optimization (procedures)
- synthesis of VHDL statements
- verification