STAND-ALONE PROJECT

FINAL REPORT

Project number	**P21694**
Project title	**Modeling Fault-Tolerant Asynchronous Logic (FATAL)** **Modellierung Fehlertoleranter Asynchroner Logik (FATAL)**
Project leader	**Ulrich Schmid, TU Wien**
Project website	**http://ti.tuwien.ac.at/ecs/research/projects/fatal**

I. Summary for public relations work

1. Zusammenfassung für die Öffentlichkeitsarbeit

Ziel des FATAL-Projekts war die Entwicklung der Grundlagen eines Frameworks für die hierarchische Modellierung und Analyse von fehlertoleranten asynchronen Very-Large Scale Integrated (VLSI) Schaltungen, zusammen mit der experimentellen Untersuchung von strahlungsinduzierten Fehlern und Metastabilität. FATAL war ein gemeinsames Projekt des Instituts für Technische Informatik (E182) und des Instituts für Electrodynamics, Microwave and Circuit Engineering (E354) der TU Wien.

Moderne VLSI-Chips werden zunehmend als lose gekoppelte Systeme interagierender Subsysteme (Systems-on-Chip) betrachtet, die viele Gemeinsamkeiten mit jenen verteilten Systemen haben, die seit Jahrzehnten unter dem Schlagwort fehlertolerante Systeme erforscht werden. In FATAL wurden einige der existierenden Berechnungs- und Fehlermodelle, Algorithmen & Protokolle und theoretischen Resultate für den VLSI-Kontext adaptiert und, wo erforderlich, neue Instanzen geschaffen. Die Hauptergebnisse sind:

(1) Ein neues zeitkontinuierliches, wertdiskretes Modellierungs- und Analyse-Framework für asynchrone VLSI-Schaltungen. Anstatt auf zeitdiskreten Zustandsübergängen basiert es auf kontinuierlicher Berechnung, unterstützt hierarchische Komposition/Dekomposition von Modellen und Implementierungen und erlaubt modulare Korrektheitsbeweise auf niedriger Abstraktionsebene. In scharfem Kontrast zur derzeitigen Praxis im VLSI-Design werden Fehler als „normal“ betrachtet und formal durch erlaubte Abweichungen vom korrekten Verhalten, einem geeigneten Fehlermodell entsprechend, spezifiziert.

(2) Durch ionisierende Teilchen in den Transistoren eines VLSI Chips erzeugte Single-Event Transients (SETs) dominieren mittlerweile die Fehlerraten. Ein substantieller Teil von FATAL war daher der Messung und Modellierung von SETs gewidmet: Spezielle on-chip Meßverstärker wurden dazu verwendet, um die detaillierten SET-Pulsformen in typischen Zielstrukturen (wie Invertern und Muller C-Gates) in Microbeam-Strahlungsexperimenten zu erfassen. Die Resultate wurden für die Kalibrierung einer detaillierten physikalischen Simulation und eines analogen Simulationsmodells mit „double-exponential“ SET-Injektion herangezogen. Letzteres wurde für die Validierung des Designs eines umfangreichen digitalen ASICs für das Langzeit-Monitoring von SETs verwendet.

(3) Ein unvermeidbares Problem in asynchronen digitalen Schaltungen ist Metastabilität, die in der Unmöglichkeit der präzisen zeitlichen Ordnung von Zustandsübergängen in verschiedenen Teilen einer Schaltung begründet ist. Im Falle eines speichernden Elements kann das zu nicht definierten Zwischenzuständen oder schneller Oszillation führen. Ein substantieller Teil von FATAL war daher der experimentellen Untersuchung

von Metastabilität in moderner VLSI-Technologie und der Frage nach einer möglichen Einbettung in das rein digitale FATAL Modellierungs- und Analyse-Framework gewidmet.

In allen diesen Gebieten konnten beträchtliche wissenschaftliche Fortschritte erzielt werden, die im Rahmen zweier kürzlich bewilligter Folgeprojekte weiter verfolgt werden.

2. Summary for public relations work

The aim of the FATAL project was the development of the foundations of a framework for the hierarchical modeling and analysis of fault-tolerant asynchronous very-large scale integrated (VLSI) circuits, in conjunction with the experimental study of radiation-induced failures and metastability. FATAL was a joint project of the Institute of Computer Engineering (E182) and the Institute of Electrodynamics, Microwave and Circuit Engineering (E354) at TU Vienna.

Modern VLSI chips are increasingly considered as more or less loosely-coupled systems of interacting subsystems (Systems-on-Chip), which have much in common with the distributed computing systems that have been studied by the fault-tolerant distributed systems community for decades. In FATAL, we utilized/adapted some of the existing computing and failure models, algorithms & protocols, and theoretical results regarding solvability of problems and achievable performance in the VLSI context, and created specifically tailored new instances where needed. The major accomplishments of FATAL are:

(1) A novel continuous-time, discrete-value modeling and analysis framework specifically designed for fault-tolerant asynchronous circuits. Rather than on discrete zero-time state transitions, it is based on continuous computations, supports hierarchical composition and decomposition of models and implementations, and modular correctness proofs at low abstraction levels. In sharp contrast to the current practice in VLSI design, failures are considered part of “normal” operation, and formally captured by allowing the behavior of a faulty circuit to deviate from its specification, according to some failure model.

(2) Given that single-event transients (SETs), caused by ionizing particles hitting the transistors of a VLSI circuit, are the dominant source of errors in nanometer technology, substantial efforts in FATAL were devoted to SET measurement and modeling activities: Specifically designed on-chip analog sense amplifiers were used for the low-intrusive measurement of the detailed SET voltage pulse shapes occurring in typical digital target circuits (such as inverters and Muller C-gates) in micro-beam irradiation experiments. The results were used for calibrating a detailed physical circuit simulation and a double-exponential SET-injection-based analog simulation model. The latter has been used for the validation of the design of a comprehensive digital SET long-term monitoring ASIC.

(3) An inevitable problem in asynchronous digital circuits is metastability, which originates in the inability to always determine the precise order of state transitions occurring in different parts of a circuit. In case of a state-holding device like a memory cell, this could

lead to intermediate-valued states or fast oscillations. A substantial part of FATAL has been devoted to the experimental evaluation of metastability generation in modern VLSI technology, as well as to identifying ways of incorporating it in our all-digital FATAL modeling and analysis framework.

We are happy to say that we made substantial scientific progress in all these major areas in FATAL, and will be able to continue our efforts in two recently granted FWF projects.

II. Brief project report

1. Report on research work

1.1 Information on the development of the research project

FATAL primarily consisted of 3 main tracks. Whereas the actual work conducted in these tracks was reasonably independent from each other, and required very different solution approaches, their final outcomes are complementary in that they have been/will eventually be integrated into a comprehensive modeling & analysis framework.

(1) **FATAL modeling and analysis framework:** We developed a generic framework [11] that supports the hierarchical modeling and analysis of fault-tolerant digital VLSI circuits. Using a behavioral approach that entirely focuses on the continuous-time, discrete-value input and output signals of a module, it allows composition/decomposition of module specifications and implementations, and supports fault-tolerance by allowing faulty modules to deviate from their correct behaviors according to some fault model. Our framework has successfully been applied for proving correct several variants of our Byzantine fault-tolerant distributed clock generation schemes DARTS and FATAL$^+$ [9].

(2) **SET modeling and experiments:** Since single-event transients (SETs), caused by ionizing particles hitting the transistors of a VLSI circuit, are the dominant source of errors in nanometer VLSI technology, substantial efforts in FATAL were devoted to SET measurement and modeling, at multiple levels [28]: We provided an accurate analog (HSpice) SET generation model[1], which has been calibrated by means of 3D TCAD (Cadence) simulation models of custom target circuits (such as inverters and Muller C-gates). Since manufacturers do not disclose relevant details like doping profiles, however, we had to resort to TCAD model validation my means of SET measurements in manufactured versions (UMC 90nm bulk CMOS technology) of our circuits: Specifically designed on-chip analog sense amplifiers were used for the low-intrusive measurement of the detailed SET voltage pulse shapes occurring in various micro-beam irradiation experiments [10], primarily conducted at the GSI in Darmstadt. The calibrated analog simulation models have been used for assessing a variety of radiation-tolerant digital circuit designs [19]-[24].

(3) **Metastability modelling and experiments:** An inevitable problem in asynchronous digital circuits is metastability, which originates in the inability to always determine the precise order of state transitions occurring in different parts of a circuit. In case of a state-holding device like a memory cell, this could lead to intermediate-valued states or fast

[1] This model will be refined in our successor project EASET (P26435), which will use our unique on-chip measurement approach to investigate subtle details of SET generation (like charge sharing) in nanometer VLSI technology.

oscillations. This track of FATAL has been devoted to the experimental evaluation of metastability generation in modern VLSI technology [34], as well as to identifying ways[2] of incorporating it in our all-digital FATAL modeling and analysis framework.

We are happy to say that we made substantial scientific progress in all these tracks, which is witnessed by 6 reviewed journal and 36 reviewed conference proceedings publications, 6 non-reviewed publications, 4 submitted/accepted journal papers, 4 PhD theses, 7 Master theses, and 2 recently granted FWF successor projects.

FATAL was a joint project between the Institute of Computer Engineering (E182) and the Institute of Electrodynamics, Microwave and Circuit Engineering (E354) at TU Vienna, as witnessed by 3 joint journal and 4 joint conference publications, and involved strong external collaborations as well. Overall, the FATAL project evolved as expected, except for the SET experiments in Track (2), where two unexpected problems forced us to adjust our goals and work plan in the course of the project (detailed in Section 1.3 below).

1.2 Most important results and brief description of their significance

(1) FATAL modeling and analysis framework: We developed the very first continuous-time discrete-value modeling & analysis framework[3] for fault-tolerant asynchronous digital circuits [11][N7], and applied it to variants of our DARTS fault-tolerant clock generation scheme [5][1]. Subsequently, in an external collaboration with Christoph Lenzen and Danny Dolev (Hebrew U. Jerusalem), we started exploring the challenging problem of adding self-stabilization to the picture, leading to the very first self-stabilizing and Byzantine fault-tolerant distributed clock generation scheme FATAL$^+$ [9] and the clock distribution grid HEX [29].

As a byproduct of the main work in this track, we also established an interesting connection between handshaking in asynchronous circuits and link reversal protocols [6], which was driven by an external collaboration with Bernadette Charron-Bost (Ecole Polytechnique Paris) and Jennifer Welch (Texas A&M U.). Last but not least, work conducted in this track of FATAL also led to interesting designs of robust asynchronous circuits [32][N10][N8].

(2) SET modeling and experiments: Using the analog circuit design competence of E354, we developed the layout as well as matching analog and 3D TCAD simulation models for (i) several target circuits, including Muller C-Gates, and (ii) high-bandwidth low-intrusive analog sense amplifiers for the on-chip measurement of SET voltage pulses (in UMC 90 nm CMOS technology) [12]. A number of small test chips with different target circuits (inverter chains,

[2] Proceeding along this way, i.e., actually incorporating a fully-fledged digital metastability generation and propagation model in our modeling and analysis framework will be done in our successor project SIC (P26436), which also adds self-stabilization to the picture. Thanks to the foundational work conducted in FATAL, we were able to quickly make progress here, as witnessed by a recently accepted JACM publication [44] and a JCSS publication [45].

[3] Such a framework was identified as lacking in the Dagstuhl seminar 08371 *Fault-tolerant Distributed Algorithms on VLSI Chips* [N2] co-organized by the project leader.

elastic pipelines) and on-chip sense amplifiers attached to several circuit nodes have been produced by UMC via IMEC ASIC service. Since the 50Ω output of our amplifiers can directly drive a channel of a fast real-time sampling oscilloscope, the latter could be used for SET recording in micro-beam experiments. Using additional funding from TU Vienna, we were able to build-up and continuously improve an elaborate (but portable) measurement setup for such experiments.

In an external collaboration with Kay-Obbe Voss at the micro-beam facility of the GSI in Darmstadt [N4], we performed several irradiation experiments, with different heay ions [12][10]. Another measurement campaign took place in collaboration with Ulrich Giesen at the PTB in Braunschweig [N5], using Alpha-particles [27][39]. The SET pulse shapes recorded in these experiments were employed for calibrating the doping profiles of our TCAD models, which incorporate SRIM nuclear codes for simulating particle strikes of different LETs. Most simulations have executed at the Vienna Scientific Cluster [N6].

The predictions by the TCAD models, in turn, have been used to calibrate a standard double-exponential SET injection analog model. Using the latter, we finally assessed the SET robustness of a number of different target circuit structures [20][22][23][38]. In addition, we developed the complete design of the FRad chip (best paper award DSD'12 [19], invited journal paper [28]), which combines several different instances of these target circuits with a unique radiation-tolerant architecture [21][24][42] and off-chip interface [14] for long-term SET monitoring.

The detailed analog SET pulses obtained in our experiments also allowed us to address the question of modeling accuracy of the standard double-exponential analog SET model. Since several deficiencies were found [33][40][38] in simulation studies, partly in a collaboration with Lorena Anghel (TIMA Labs Grenoble), developing better analog models will be a core research topic in our follow-up FWF project EASET.

(3) Metastability modelling and experiments: We used the detailed analog (HSpice) simulation models of the Muller C-Gates developed in Track (2), as well as circuit structures from the UMC 90 nm standard library, for simulation experiments assessing the effect of Schmitt-triggers [18] on metastability generation. Our experiments used the metastability test ASICs developed by E354, which also contain a custom tuneable delay line [13] needed for generating metastable upsets. For standard circuit structures such as flip-flops and latches, we resorted to FPGA-based experiments [34]. Using our setup, we characterized metastable upsets of Muller C-Gates [36][46] and latches [35] in an all-digital fashion [N9].

Apart from this bottom-up approach, which aimed at an all-digital modeling of metastable upsets in modern VLSI technology, some efforts have also been spent on a top-down approach that starts out from problems like the impossibility to implement a perfect arbiter.

We established the remarkable result that none of the existing continuous-time binary-value circuit models allows to faithfully model glitch propagation [31].

1.3 Information on the execution of the project, use of available funds and any changes to the original project plan

FATAL project duration: October 2009 – March 2014 (cost-neutral extension by 18 months)

not funded by the FWF			**funded by the FWF (project)**		
co-workers	**Number**	**Person-months**	**co-workers**	**number**	**Person - months**
non-scientific co-workers			non-scientific co-workers		
diploma students	2	12	diploma students	3	25
PhD students	3	85	PhD students	5	94
post-doctoral co-workers	2	15	post-doctoral co-workers		
co-workers with “Habilitation” (professorial qualifications)	1	8	co-workers with “Habilitation” (professorial qualifications)		
professors	2	15	professors		

Equipment purchased: FATAL money was only used for ASIC and PCB manufacturing costs and electronics components.

Deviations from original proposal: Our original plan was to develop both a comprehensive digital long-term SET monitoring ASIC (the FRad chip) for directly validating digital radiation failure model candidates for asynchronous circuits, and a custom ASIC for metastability experiments (the FMeta chip). However, in the course of the project, we faced the following two unexpected problems:

(1) The project originally foresaw the development of 4 ASICS (in the context of the EU Europractice project, which granted academic institutions cheap access to tools and chip

manufacturers), with a total budget of 50 kEUR. Due to the initial cut of the budget (the grant was cut by 10% = about 50 kEUR), we had to reduce our ambitions a priori here. Given this, it was hence particularly unfortunate that Europractice reached the end of its funding period by 2011 and was not seamlessly renewed. Owing to this, manufacturing costs have more than doubled: The FRad chip would have cost EUR 25.000,– rather than 5.000 - 10.000,– .

(2) For the FATAL irradiation experiments, we initially planned to use a Cf-252 vacuum chamber at our Atomic Institute, which was under construction by the time of the proposal writing. In 2011, however, we had to accept the (unexpected) fact the supplier eventually denied delivery of the requested Cf-252 radiation source. This forced us to go for accelerator-based radiation experiments.

The cost issue (1) forced us to drop manufacturing the expensive FRad and FMeta ASICs within FATAL, and rather build small test ASICs for very specific experiments instead. At the same time, the greatly improved controllability of the micro-beam experiments resorted to for compensating the unavailability of the originally foreseen Cf-252 vacuum chamber (2) allowed us to consider a different approach, namely, model validation using intermediate TCAD and analog SET models, calibrated by means of direct SET measurements using on-chip analog amplifiers. Although we had to completely change our experimental setup for this purpose, substantial additional funding from TU Vienna for building up the required measurement infrastructure allowed us to proceed in this direction. Overall, we can say that this “forced” change of our original plans resulted in significantly improved project results.

2. Personnel development – Importance of the project for the research careers of those involved

Nonwithstanding the general difficulty of assessing scientific recognition, we can safely say that the work on FATAL was very important for increasing the international reputation of our institutes: It allowed the Embedded Computing Systems Group E182/2 to further increase the visibility of its integration of fault-tolerant distributed algorithms knowledge and asynchronous digital design competence, whereas it helped E354 to become recognized in the radiation community for its expertise in on-line SET measurements.

For the individual project members, FATAL provided the following benefits:

- For the project leader *Ulrich Schmid*, FATAL was particularly important for further increasing his reputation in the area fault-tolerant distributed algorithms in systems-on-chip [N2]. For the co-project leader *Horst Zimmermann*, FATAL was an important step for further broadening the profile of his analog design group. Viewed from the global

perspective of TU Vienna, FATAL (and the follow-up project EASET) constitutes an impressive success story of a synergetic collaboration between different faculties.

- For *Andreas Steininger*, who is associate professor at E182/2 and an expert in dependable asynchronous circuit design, FATAL was instrumental for gaining recognition in radiation-tolerant circuit design. He is now project leader of the successor FWF project EASET.
- FATAL was a pivotal driver for the work conducted by *Matthias Függer*, who wrote a PhD thesis on distributed computing in digital circuits [N7], supervised by Ulrich Schmid and Jennifer Welch (Texas A&M University). He also took the lead of the dynamic systems analysis part of the work in Track (1). He is now project leader of the successor FWF project SIC.
- The FATAL project was a most inspiring and stimulating opportunity for *Jakob Lechner* to write his PhD thesis [N10] on robust GALS circuits, supervised by Andreas Steininger and Jans Sparso (DTU Kopenhagen), as this work incorporates models and techniques from both Track (2) and Track (3). After a research stay at U. Newcastle (Alex Yakovlev), he recently joined RUAG Space Austria.
- For *Syed Rameez Naqvi*, a student of TU Vienna's PhD School of Informatics, FATAL was a source of inspiration and knowledge for his PhD thesis [N8] devoted to fault-tolerant asynchronous routing in NoCs, supervised by Andreas Steininger. He is now Assistant Professor at the COMSATS Institute of Information Technology (Wah Campus) in Pakistan.
- For *Thomas Polzer*, the winner of TU Vienna's "Distinguished Young Alumnus" for his Master thesis [N11] and task leader for the metastability experiments in Track (3), FATAL was instrumental to write his PhD thesis [N9], supervised by Andreas Steininger and Alex Yakovlev (U. Newcastle). He is currently assistant professor at E182/2 and quickly gaining international recognition for this work.
- *Michael Hofbauer* was involved in the design of the FATAL test ASICS (principal designer: *Kurt Schweiger*), and primarily responsible for conducting the irradiation experiments for SET measurements and the subsequent TCAD model calibration. He will finish his PhD thesis on this topic in the context of the EASET project, under the supervision of Horst Zimmermann.
- For *Varadan Savulimedu Veeravalli*, who joined the FATAL project after his MSc at Rutgers U., FATAL was an ideal environment to apply his excellent skills in circuit design and simulation evaluation. He is the main architect of the FRad chip, and has quickly gained international recognition in the radiation-tolerant circuit architecture community.

He has been visiting researcher at TIMA Lab in Grenoble and RUAG Space Austria, and is about to finish his PhD thesis under the supervision of Andreas Steininger. He will continue his work as a PostDoc in the EASET project.

- FATAL also helped some of our Master students to make their first steps in scientific working. *Andreas Dielacher* [N13], *Markus Posch* [N14] and *Markus Hofstätter* [N16] managed to publish scientific papers about their thesis topics and are now working in industry. The same is true for *Martin Perner* [N17], who joined E182/2 as an Assistant Professor and is now working on his PhD thesis in the context of the follow-up FWF project SIC. *Thomas Nowak* [N12] joined Bernadette Charron-Bosts group at Ecole Polytechnique Paris for a PhD thesis. At E354, *Alexander Grill* did his master thesis on calibration of doping profiles for semiconductor simulation.

3. Effects of the project beyond the scientific field

FATAL was instrumental to provide transdisciplinary input into two different areas of research: (i) Further advertising the benefits of migrating fault-tolerant distributed algorithms to digital integrated circuits [N2], and (ii) transferring related expertise to the formal verification community, primarily in the context of the NFN RiSE (S11405, where the project leader is a regular PI). Some of the results of FATAL are also taught in advanced courses (like 182.703 Problems in Distributed Computing[4]) in our computer engineering Master program. Experience tells that this is a very effective means for educating students for current and future research projects.

Given the quite specialized and theoretical nature of FATAL, we cannot report any public relation-related activities within the project.

4. Other important aspects

Results obtained in FATAL were presented in talks & posters at many scientific conferences:

- Regular presentations: [1][2][3][4][5][6][7][8][9][14][15][16][17][18][19][20][21][22][23] [24][26] [27][29][30][31][32][33][34][35][36][37][38][40][42]
- Posters: [25][39][41]
- Invited talks: [N2][N3]

Members of the FATAL project chaired or organized the following related scientific events:

[4] Course web page: *http://ti.tuwien.ac.at/ecs/teaching/courses/prdc/*

- Andreas Steininger: PC Co-chair ASYNC'14, General Vice Chair DDECS'10, DDECS'11
- Ulrich Schmid: Co-organizer of RiSE Winter School in Verification 2013

Awards received by FATAL members:

- Thomas Polzer: Distinguished Young Alumnus EPILOG TU Vienna 2009 [N11]
- Martin Perner: Finalist (Top-4 Master theses) EPILOG TU Vienna 2013 [N17]
- Best paper award DSD'12 [19]
- Invited journal paper [28]

III. Attachments

1. Scholarly / scientific publications

1.1 **Peer-reviewed publications / already published** (journals, monographs, anthologies, contributions to anthologies, proceedings, research data, etc.)

[1] Andreas Dielacher, Matthias Fuegger, and Ulrich Schmid. Brief announcement: How to speed-up fault-tolerant clock generation in VLSI systems-on-chip via pipelining. In Proceedings of the 28th ACM Symposium on Principles of Distributed Computing (PODC'09), page 423. ACM Press, August 2009. An extended version is available as RR 15/2009, Institut für Technische Informatik, TU-Wien, http://www.vmars.tuwien.ac.at/documents/extern/2571/techreport.pdf.

[2] Gottfried Fuchs, Matthias Fuegger, and Andreas Steininger. On the threat of metastability in an asynchronous fault-tolerant clock generation scheme. In 15th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC'09), pages 127–136, Chapel Hill, N. Carolina, USA, May 2009.

[3] Matthias Fuegger, Gottfried Fuchs, Ulrich Schmid, and Andreas Steininger. On the stability and robustness of non-synchronous circuits with timing loops. 3rd Workshop on Dependable and Secure Nanocomputing, Jun. 2009.

[4] Thomas Polzer, Thomas Handl, and Andreas Steininger. A metastability-free multi-synchronous communication scheme for SoCs. In Stabilization, Safety, and Security of Distributed Systems, 11th International Symposium, SSS 2009, Lyon, France, November 3-6, 2009. Proceedings, pages 578–592, 2009.

[5] Matthias Függer, Andreas Dielacher, and Ulrich Schmid. How to speed-up fault-tolerant clock generation in VLSI systems-on-chip via pipelining. In Proceedings Eighth European Dependable Computing Conference (EDCC'10), pages 230–239, 2010.

[6] Bernadette Charron-Bost, Matthias Függer, Jennifer L. Welch, and Josef Widder. Full reversal routing as a linear dynamical system. In 18th International Colloquium on Structural Information and Communication Complexity (SIROCCO), LNCS, pages 101–112, Berlin, Heidelberg, 2011. Springer-Verlag.

[7] Bernadette Charron-Bost, Matthias Függer, Jennifer L. Welch, and Josef Widder. Partial is full. In 18th International Colloquium on Structural Information and Communication Complexity (SIROCCO), LNCS, 2011.

[8] Bernadette Charron-Bost, Matthias Függer, Jennifer L. Welch, and Josef Widder. Brief announcement: Full reversal routing as a linear dynamical system. In Proceedings SPAA, 2011.

[9] Danny Dolev, Matthias Függer, Christoph Lenzen, and Ulrich Schmid. Fault-tolerant algorithms for tick-generation in asynchronous logic: Robust pulse generation [extended abstract]. In Proceedings 13th International Symposium on Stabilization, Safety, and Security of Distributed Systems (SSS'11), Springer LNCS 6976, pages 163–177, 2011.

[10] Michael Hofbauer, Kurt Schweiger, Horst Dietrich, Horst Zimmermann, Kay-Obbe Voss, Bruno Merk, Ulrich Schmid, and Andreas Steininger. Pulse shape measurements by on-chip sense amplifiers of single event transients propagating through a 90 nm bulk CMOS inverter chain. IEEE Transactions on Nuclear Science, 59(6):2778–2784, December 2012.

[11] Matthias Függer and Ulrich Schmid. Reconciling fault-tolerant distributed computing and systems-on-chip. Distributed Computing, 24(6):323–355, 2012. http://www.springer.com/alert/urltracking.do?id=L4fc2b9M93e09eSaf96e87

[12] K. Schweiger, M. Hofbauer, H. Dietrich, H. Zimmermann, K.O. Voss, and B. Merk. Position dependent measurement of single event transient voltage pulse shapes under heavy ion irradiation. Electronics Letters, 48(3):171–172, 2012.

[13] S. Schidl, K. Schweiger, W. Gaberl, and H. Zimmermann. Analogously tunable delay line for on-chip measurements with sub-picosecond resolution in 90 nm CMOS. Electronics Letters, 48(15):910 –911, 7 2012.

[14] Bernhard Fritz, Varadan Savulimedu Veeravalli, and Andreas Steininger. Reliable gateway for radiation experiments on a VLSI chip. In Proceedings Austrochip 2012, pages 65–70, Oct. 2012.

[15] Jakob Lechner. Designing robust GALS circuits with triple modular redundancy. 2012 European Dependable Computing Conference (EDCC), May. 2012.

[16] Jakob Lechner and Martin Lampacher. Protecting pipelined asynchronous communication channels against single event upsets. In 2012 IEEE 30th International Conference on Computer Design, Sept. 2012, 2012.

[17] Jakob Lechner, Martin Lampacher, and Thomas Polzer. A robust asynchronous interfacing scheme with four-phase dual-rail coding. 2012 International Conference on Application of Concurrency to System Design (ACSD), Jun. 2012.

[18] Thomas Polzer, Andreas Steininger, and Jakob Lechner. Muller C-elements metastability containment. In International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS) 2012, Sept. 2012, 2012.

[19] Varadan Savulimedu Veeravalli, Thomas Polzer, Andreas Steininger, and Ulrich Schmid. Architecture and design analysis of a digital single-event transient/upset measurement chip. In Proceedings 15th Euromicro Symposium on Digital System Design: Architectures, Methods and Tools (DSD'12), pages 8–17, Sep. 2012. (**Best paper award**).

[20] Varadan Savulimedu Veeravalli and Andreas Steininger. Radiation-tolerant combinational gates: An implementation based comparison. In Proceedings 15th IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS'12), pages 115–120, Apr. 2012.

[21] Varadan Savulimedu Veeravalli and Andreas Steininger. Architecture for monitoring set propagation in 16-bit Sklansky adder. In 15th International Symposium on Quality Electronics Design (ISQED'14), pages 412–419, Mar. 2014.

[22] Varadan Savulimedu Veeravalli and Andreas Steininger. Efficient radiation-hardening of a Muller C-element. In Proceedings 2012 Single Event Effects Symposium, Apr. 2012.

[23] Varadan Savulimedu Veeravalli and Andreas Steininger. Monitoring single event transient effects in dynamic mode. In 1st Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale (MEDIAN'12), pages 51–54, June 2012.

[24] Varadan Savulimedu Veeravalli and Andreas Steininger. LFSR implementation using C-elements. In Proceedings MEMICS 2012, pages 73–83, Oct. 2012.

[25] Michael Hofbauer, Kurt Schweiger, Horst Dietrich, Horst Zimmermann, Kay-Obbe Voss, Bruno Merk, Ulrich Schmid, and Andreas Steininger. Pulse shape measurements by on-chip sense amplifiers of single event transients propagating through a 90 nm bulk CMOS inverter chain, 2012. Poster at IEEE Nuclear and Space Radiation Effects Conference (NSREC'12), Miami (USA).

[26] Michael Hofbauer, Kurt Schweiger, Horst Zimmermann, Ulrich Giesen, Frank Langner, Ulrich Schmid, and Andreas Steininger. Supply voltage dependent on-chip single event transient pulse shape measurements in 90 nm bulk CMOS under alpha irradiation. In Proceedings 21st

European Conference on Radiation and its Effects on Components and Systems (RADECS'12), Sep. 2012.

[27] Michael Hofbauer, Kurt Schweiger, Horst Zimmermann, Ulrich Giesen, Frank Langner, Ulrich Schmid, and Andreas Steininger. Supply voltage dependent on-chip single event transient pulse shape measurements in 90 nm bulk CMOS under alpha irradiation. IEEE Transactions on Nuclear Science, 60(4):2640–2646, August 2013.

[28] Varadan Savulimedu Veeravalli, Thomas Polzer, Andreas Steininger, Ulrich Schmid, Michael Hofbauer, Kurt Schweiger, Horst Dietrich, Kerstin Schneider-Hornstein, Horst Zimmermann, Kay-Obbe Voss, Bruno Merk, and Michael Hajek. An infrastructure for accurate characterization of single-event transients in digital circuits. Microprocessors and Microsystems, 37(8-A):772–791, 2013. http://www.sciencedirect.com/science/article/pii/S0141933113000598

[29] Danny Dolev, Matthias Függer, Christoph Lenzen, Martin Perner, and Ulrich Schmid. HEX: Scaling Honeycombs is Easier than Scaling Clock Trees. In Proc. 25th ACM Symp. on Parallelism in Algorithms and Architect ures (SPAA'13), pages 164–175, 2013.

[30] Matthias Függer, Markus Hofstätter, Christoph Lenzen, and Ulrich Schmid. Efficient construction of global time in SoCs despite arbitrary faults. In Proc. 16th Euromicro Conference on Digital System Design (DSD'13), pages 142–151, 2013.

[31] Matthias Függer, Thomas Nowak, and Ulrich Schmid. Unfaithful glitch propagation in existing binary circuit models. In Proceedings 19th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC'13), pages 191–199. IEEE Computer Society, 2013.

[32] Jakob Lechner and Varadan Savulimedu Veeravalli. Modular redundancy in a GALS system using asynchronous recovery links. In 19th IEEE International Symposium on Asynchronous Circuits and Systems, May 2013, 2013.

[33] Robert Najvirt, Varadan Savulimedu Veeravalli, and Andreas Steininger. Particle strikes in C-gates: Relevance of SET shapes. In Proceedings 2nd Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale (MEDIAN'13), 2013.

[34] Thomas Polzer and Andreas Steininger. An approach for efficient metastability characterization of FPGAs through the designer. In 19th IEEE International Symposium on Asynchronous Circuits and Systems, May 2013, 2013.

[35] Thomas Polzer and Andreas Steininger. Digital late-transition metastability simulation model. In Euromicro Conference on Digital System Design (DSD'13), pages 121–128, 2013.

[36] Thomas Polzer and Andreas Steininger. Metastability characterization for Muller C-elements. In Proceedings 23rd International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS'13), pages 164–171, 2013.

[37] Martin Perner, Martin Sigl, Ulrich Schmid, and Christoph Lenzen. Byzantine self-stabilizing clock distribution with HEX: Implementation, simulation, clock multiplication. In Proc. Sixth IARIA International Conference on Dependability (DEPEND'13), pages 6–15, 2013.

[38] Varadan Savulimedu Veeravalli and Andreas Steininger. Performance of radiation hardening techniques under voltage and temperature variations. In 2013 IEEE Aerospace Conference, March 2013, 2013.

[39] Michael Hofbauer, Kurt Schweiger, Horst Dietrich Wolfgang Gaberl, Horst Zimmermann, Ulrich Giesen, Frank Langer, Ulrich Schmid, and Andreas Steininger. Single event transient pulse shape measurements by on-chip sense amplifiers in a single inverter for intermediate input states under alpha irradiation, 2013. Poster at IEEE Nuclear and Space Radiation Effects Conference (NSREC'13).

[40] Lorena Anghel, Varadan Savulimedu Veeravalli, Dan Alexandrescu, Andreas Steininger, Kerstin Schneider-Hornstein, and Enrico Costenaro. Single event effects in Muller C-elements and asynchronous circuits over a wide energy spectrum. In Proceedings 10th IEEE Workshop on Silicon Errors in Logic -System Effects (SELSE'14), 2014.

[41] Varadan Savulimedu Veeravalli and Andreas Steininger. Poster: Diagnosis of SET propagation in combinational logic under dynamic operation. In Proceedings 10th IEEE Workshop on Silicon Errors in Logic -System Effects (SELSE'14), 2014.

[42] Varadan Savulimedu Veeravalli, Andreas Steininger, and Ulrich Schmid. Measuring set pulsewidths in logic gates using digital infrastructure. In Proceedings Internationsal Symposium on Quality of Electronic Design (ISQED'14), 2014.

1.2 Non peer-reviewed publications / already published (journals, monographs, anthologies, contributions to anthologies, research reports, working papers / preprints, proceedings, research data, etc.)

[N1] Andreas Dielacher, Matthias Függer, and Ulrich Schmid. How to speedup fault-tolerant clock generation in VLSI systems-on-chip via pipelining. Research Report 15/2009, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 1-3/182-1, 1040 Vienna, Austria, 2009. http://www.vmars.tuwien.ac.at/documents/extern/2571/techreport.pdf.

[N2] Bernadette Charron-Bost, Shlomi Dolev, Jo Ebergen, and Ulrich Schmid. 08371 Summary – fault-tolerant distributed algorithms on VLSI chips. In Bernadette Charron-Bost, Shlomi Dolev, Jo Ebergen, and Ulrich Schmid, editors, Fault-Tolerant Distributed Algorithms on VLSI Chips, number 08371 in Dagstuhl Seminar Proceedings, Dagstuhl, Germany, 2009. Schloss Dagstuhl -Leibniz-Zentrum fuer Informatik, Germany. http://drops.dagstuhl.de/opus/frontdoor.php?source opus=1927.

[N3] Danny Dolev, Matthias Fuegger, Christoph Lenzen, and Ulrich Schmid. Towards self-stabilizing byzantine fault-tolerant clock generation in systems-on-chip. In 2012 NITRD National Workshop on the New Clockwork for Time-Critical Systems, October 25-26, Baltimore (USA), Oct. 2012.

[N4] Michael Hofbauer, Kurt Schweiger, Horst Dietrich, Horst Zimmermann, Ulrich Schmid, and Bruno Merk. Single event effect measurements in 90nm CMOS circuits at the microbeam facility for the project FATAL. In GSI Scientific Report 2011, page 424, GSI Helmholtzzentrum für Schwerionenforschung GmbH, Darmstadt, Germany, 2012.

[N5] Michael Hofbauer, Kurt Schweiger, Horst Dietrich, Horst Zimmermann, Ulrich Schmid, and Ulrich Giesen. Messung der Auswirkungen von ionisierender Strahlung auf 90 nm CMOS Schaltungen. Technical report, Physikalisch Technische Bundesanstalt, 2012.

[N6] Michael Hofbauer, Kurt Schweiger, Horst Zimmermann, and Ulrich Schmid. Projekt FATAL, 2012. Vienna Scientific Cluster Brochure 2012, p. 53.

PhD and Master theses:

[N7] Matthias Függer. Analysis of On-Chip Fault-Tolerant Distributed Algorithms. PhD thesis, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 3/3/182-2, 1040 Vienna, Austria, 2010.

[N8] Syed Rameez Naqvi. A Non-Blocking Fault-Tolerant Asynchronous Networks-on-Chip Router. PhD thesis, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 3/3/182-2, 1040 Vienna, Austria, 2013.

[N9] Thomas Polzer. A Digital Metastability Model for VLSI Circuits. PhD thesis, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 3/3/182-2, 1040 Vienna, Austria, 2014.

[N10] Jakob Lechner. Building Robust GALS Circuits – Fault-Tolerant and Variation-Aware Design Techniques for Reliable Circuit Operation. PhD thesis, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 3/3/182-2, 1040 Vienna, Austria, 2014.

[N11] Thomas Polzer. Fault-tolerant hardware implementation of a consensus algorithm. Master's thesis, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 3/3/182-1, 1040 Vienna, Austria, 2009.

[N12] Thomas Nowak. Topology in distributed computing. Master thesis, Embedded Computing Systems Group, Technische Universität Wien, March 2010.

[N13] Andreas Dielacher. A pipelined distributed fault-tolerant clock generation algorithm in VLSI: Proofs and implementation. Master's thesis, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 3/3/182-1, 1040 Vienna, Austria, 2010.

[N14] Markus Posch. Selbststabilisierende Byzantinisch fehlertolerante takterzeugung in FPGAs. Master's thesis, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 3/3/182-1, 1040 Vienna, Austria, 2012.

[N15] A. Grill. A framework for simulation and parameter optimization of a 90 nm CMOS process in Sentaurus. Master's thesis, Technische Universität Wien, Institute of Electrodynamics, Microwaves and Circuit Engineering, Gusshausstrasse 25/354, 1040 Vienna, Austria, 2013.

[N16] Markus Hofstätter. Solving the labeling problem: A byzantine fault-tolerant self-stabilizing FPGA prototype based on the FATAL$^+$ protocol. Master's thesis, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 3/3/182-1, 1040 Vienna, Austria, 2013.

[N17] Martin Perner. Self-stabilizing Byzantine fault-tolerant clock distribution in grids. Master's thesis, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 3/3/182-1, 1040 Vienna, Austria, 2013.

1.3 Planned publications

(journals, monographs, anthologies, contributions to anthologies, proceedings, research data, etc.)

Author(s)	[43] Matthias Függer, Thomas Nowak, and Ulrich Schmid.		
Title	Unfaithful glitch propagation in existing binary circuit models		
Sources	CoRR abs/1311.1423, 2013. Submitted to IEEE Trans.Comput.		
URL (if applicable)			
Peer Review	yes		
Status		submitted	

Author(s)	[44] Danny Dolev, Matthias Függer, Ulrich Schmid, and Christoph Lenzen.		
Title	Fault-tolerant algorithms for tick-generation in asynchronous logic: Robust pulse generation.		
Sources	Journal of the ACM, 2014		
URL (if applicable)			
Peer Review	yes		
Status	accepted		

Author(s)	[45] Danny Dolev, Matthias Függer, Christoph Lenzen, Markus Posch, Ulrich Schmid, and Andreas Steininger.		
Title	Rigorously modeling self-stabilizing fault-tolerant circuits: An ultra-robust clocking scheme for systems-on-chip.		
Sources	Journal of Computer and System Sciences, 2014.		
URL (if applicable)			
Peer Review	yes		
Status	accepted		

Author(s)	[46] Kurt Schweiger, Michael Hofbauer, Stefan Schidl, Kerstin Schneider-Hornstein, Horst Zimmermann, Thomas Polzer, Andreas Steininger.		
Title	Characterization of Deep Metastability in a 90 nm CMOS Muller-C Element by Use of On-Chip Delay Lines		
Sources	Submitted to IEEE Trans. VLSI Systems		
URL (if applicable)			
Peer Review	yes		
Status		submitted	

2. Most important academic awards

(Specific academic awards, honours, prizes, medals or other merits)

Name of award	n=national / i=international
Best paper award DSD'12 [19]	I
Invited journal MICPRO [28]	I
Thomas Polzer: Distingiushed Young Alumnus EPILOG 2009 TU Vienna	n
Martin Perner: Finalist EPILOG 2013 TU Vienna	n

3. Information on results relevant to commercial applications

None.

4. Publications for the general public and other publications

(Absolute figures, separate reporting of national / international publications)

	national	International
Self-authored publications on the www	0	0
Editorial contributions in the media	0	0
(Participatory) contributions within science communication	0	0
Popular science contributions	0	0

5. Development of collaborations

Indication of the most important collaborations (no more than 5) that took place (i.e. were initiated or continued) in the course of the project. Please provide the name of the collaboration partner (name, title, institution) and a few words about the scientific content. Please **categorise** each collaboration arrangement as follows:

N				Nationality of collaboration partner (please use the ISO-3-letter country code)
	G			Gender **F (**female) **M** (male)
		E		Extent **E1** **low** (e.g. no joint publications, but mention in acknowledgements or similar); **E2** **medium** (collaboration e.g. with occasional joint publications, exchange of materials or similar, but no longer-term exchange of personnel); **E3** **high** (extensive collaboration with mutual hosting of group members for research stays, regular joint publications, etc.)
			D	Discipline **W** **within the discipline** (within the same scientific field) **I** **interdisciplinary** (involving two or more disciplines) **T** **transdisciplinary** (collaborations outside the sciences)

N	G	E	D	Name	Institution
FRA	F	E3	I	Bernadette Charron-Bost	Ecole Polytechnique Paris
ISR	M	E3	W	Danny Dolev	Hebrew University Jerusalem
DEU	M	E3	I	Ulrich Giesen	PTB Braunschweig
US	M	E3	W	Christoph Lenzen	MIT
DEU	M	E3	I	Kay-Obbe Voss	GSI Darmstadt
FRA	F	E3	W	Lorena Anghel	TIMA Grenoble

6. Development of human resources in the course of the project

(Absolute figures with an indication of status (in progress / completed)

	In progress	Completed	Gender	
			f	m
Full professorship	0	0		
Venia thesis (*Habilitation*) / Equivalent senior scientist qualification	0	0		
Postdoc	2	0	1	1
Ph.D. theses	2	4	0	6
Master's theses	0	7	0	7
Diploma theses	0	0		
Bachelor's theses	0	0		

7. Applications for follow-up projects

(Please indicate the status of each project and the funding organisation)

7.1 Applications for follow-up projects (FWF projects)

Please indicate the project type (e.g. stand-alone project, SFB, DK, etc.)

Project number (if applicable)	**P26435**		
Project type	**Stand-alone project**		
Title / subject	**Accelerator-based Experimental Analysis and Simulation Modeling of Single-Event-Transients in VLSI Circuits (EASET)**		
Status	granted ☒	pending ☐	in preparation ☐
Application reference (if a patent is applied)			

Project number (if applicable)	**P26436**		
Project type	**Stand-alone project**		
Title / subject	**Self-stabilizing Byzantine Fault-Tolerant Distributed Algorithms for Integrated Circuits (SIC)**		
Status	granted ☒	pending ☐	in preparation ☐
Application reference (if a patent is applied)			

7.2 Applications for follow-up projects (Other national projects)

(e.g. FFG, CD Laboratory, K-plus centres, funding from the Austrian central bank [OeNB], Austrian federal government, provincial agencies, provincial government or similar sources)

None.

7.3 Applications for follow-up projects (international projects) (e.g. EU, ERC, or other international funding agencies)

None.

IV. Cooperation with the FWF

Please rate the following aspects with regard to your interaction with the FWF. Please provide any **additional comments (explanations)** on the supplementary sheet with a reference to the corresponding question/aspect.

Scale:
-2 highly unsatisfactory
-1 unsatisfactory
0 appropriate
+1 satisfactory
+2 highly satisfactory
X not used

Rules

(i.e. guidelines for: funding programme, application, use of resources, reports)

Rating

Application guidelines	Length	**+1**
	Clarity	**+2**
	Intelligibility	**+2**

Procedures (submission, review, decision)

	Advising	**X**
	Duration of procedure	**0**
	Transparency	**+1**

Project support

Advising	Availability	**+2**
	Level of detail	**+2**
	Intelligibility	**+2**

Financial transactions (credit transfers, equipment purchases, personnel management)	**+2**

Reporting / review / exploitation

	Effort	**+2**
	Transparency	**+2**
	Support in PR work / exploitation	**X**

Comments on cooperation/interaction with the FWF:

Excellent support and cooperation since many years.