Fault-Tolerant Algorithms on SoCs - A case study

A. Steininger, M. Függer, U. Schmid, G. Fuchs

The Basic Idea

- short time to market
- high circuit complexity
- high clock rates
- high logic density
- small critical charge

Can we employ distributed algorithms in SoCs?

Our approach

- Overcome the problem of designing a perfectly laid-out global clock tree, but still maintain a reasonably synchronous view.
- Partition the chip into loosely coupled functional units, together forming an SoC.
- Attach small TS-Algs (Tick Synchronization Algorithm) units to the units. The TS-Algs provide the units with local clock signals.
- Let the TS-Algs communicate via a dedicated on-chip TS-Net, allowing them to synchronize with each other and hence providing synchronized local clock signals to all units.

Project aim

- Efficient TS-Net implementation
- Algorithm adaptation for 0-bit messages
- Atomicity of actions in hardware
- Fault-tolerant handshaking

Our Results

- Algorithm adapted to cope with the challenging VLSI requirements
- Correctness formally proved and performance metrics formally derived
- Prototype implementation with promising evaluation results

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