

Fault-Tolerant Distributed Clock Generation in VLSI Systems-on-Chip

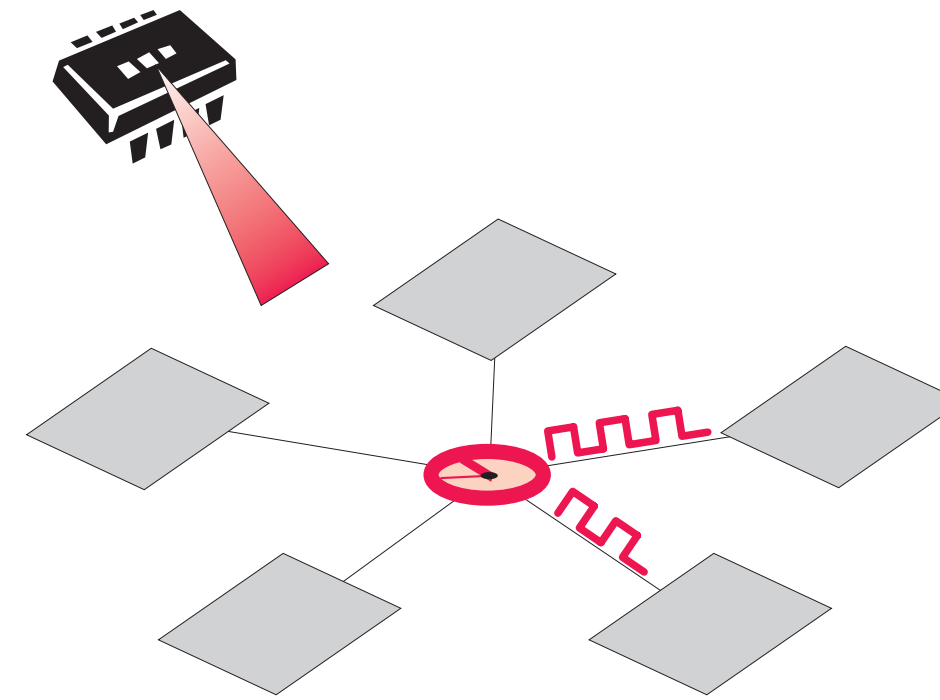
Motivation:

The concept of synchronous design:

Global notion of time for the entire chip

Achieved by the reduction of continuous time to discrete, evenly spaced time slices produced by a single oscillator.

The oscillator supplies the same clock signal to all functional units at the chip.



Conceptual problems of synchronous design methodologies:

Clock skew of up to 100%

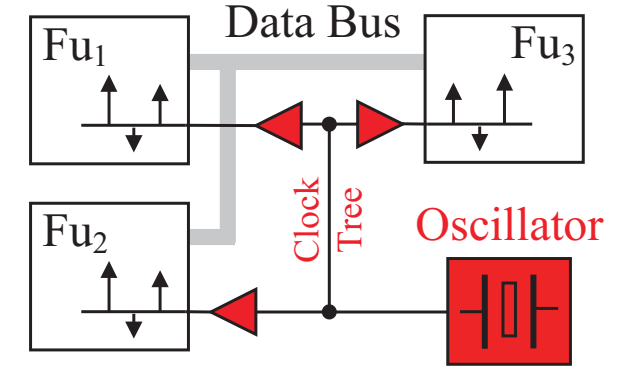
Clock tree design becomes an important design phase at today's clock frequencies (10 Ghz domain): X-Trees, H-Trees, programmable clock delays, clock buffers, ...

Reduced signal swing

To reduce the power consumption (proportional to the square of clock frequency), the signal swing is reduced → increasing risk of transient failures (single-event upsets, crosstalk).

Single point of failure

A faulty quartz oscillator may lead to a breakdown of the entire chip.



Presented Solution:

This master's thesis presents and formally proves correct an alternative to monolithic synchronous designs, which is currently investigated in the DARTS project (a cooperation between the Vienna University of Technology and Austrian Aerospace).



Photo: ESA/AOES Medialab

The DARTS Aim & Approach:

Project aim

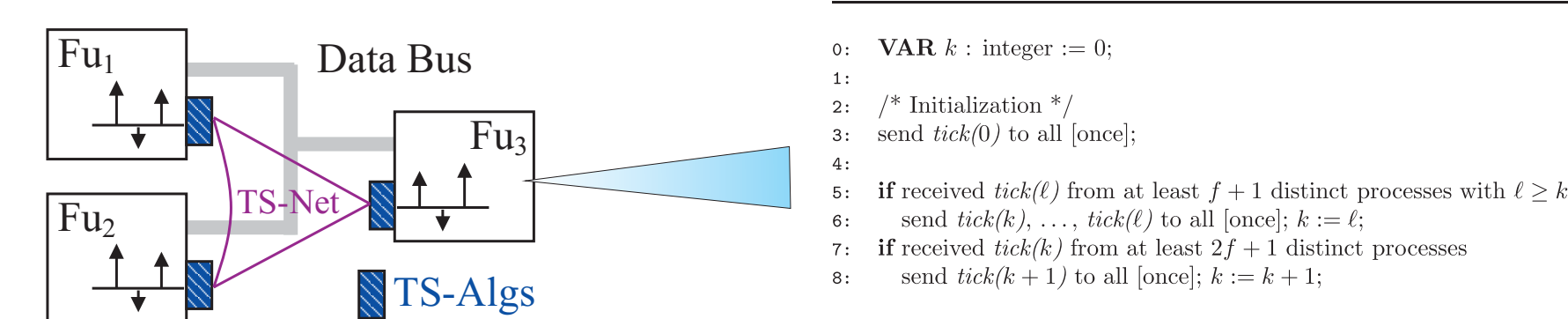
Overcome the problem of designing a perfectly laid-out global clock tree, but still maintain a reasonably synchronous view.

Our approach

(1) Partition the chip into n loosely coupled functional units Fu_i , together forming a System-on-Chip (SoC).

(2) Attach small TS-Alg (Tick Synchronization Algorithm) units to the Fu_i s. The TS-Algs provide the Fu_i s with local clock signals.

(3) Let the TS-Algs communicate via a dedicated on-chip TS-Net, allowing them to synchronize with each other and hence providing synchronized local clock signals to all Fu_i s.



Replacing synchronous clocking with fault-tolerant distributed tick generation algorithms.

Advantages of our Approach:

Fault-Tolerance

The synchronization properties (precision and accuracy) can be maintained if up to f out of $n > 3f+1$ TS-Algs fail arbitrarily.

Synchrony

Max phase-difference and max/min frequencies of local clock signals can be guaranteed (formally proved in this master's thesis).

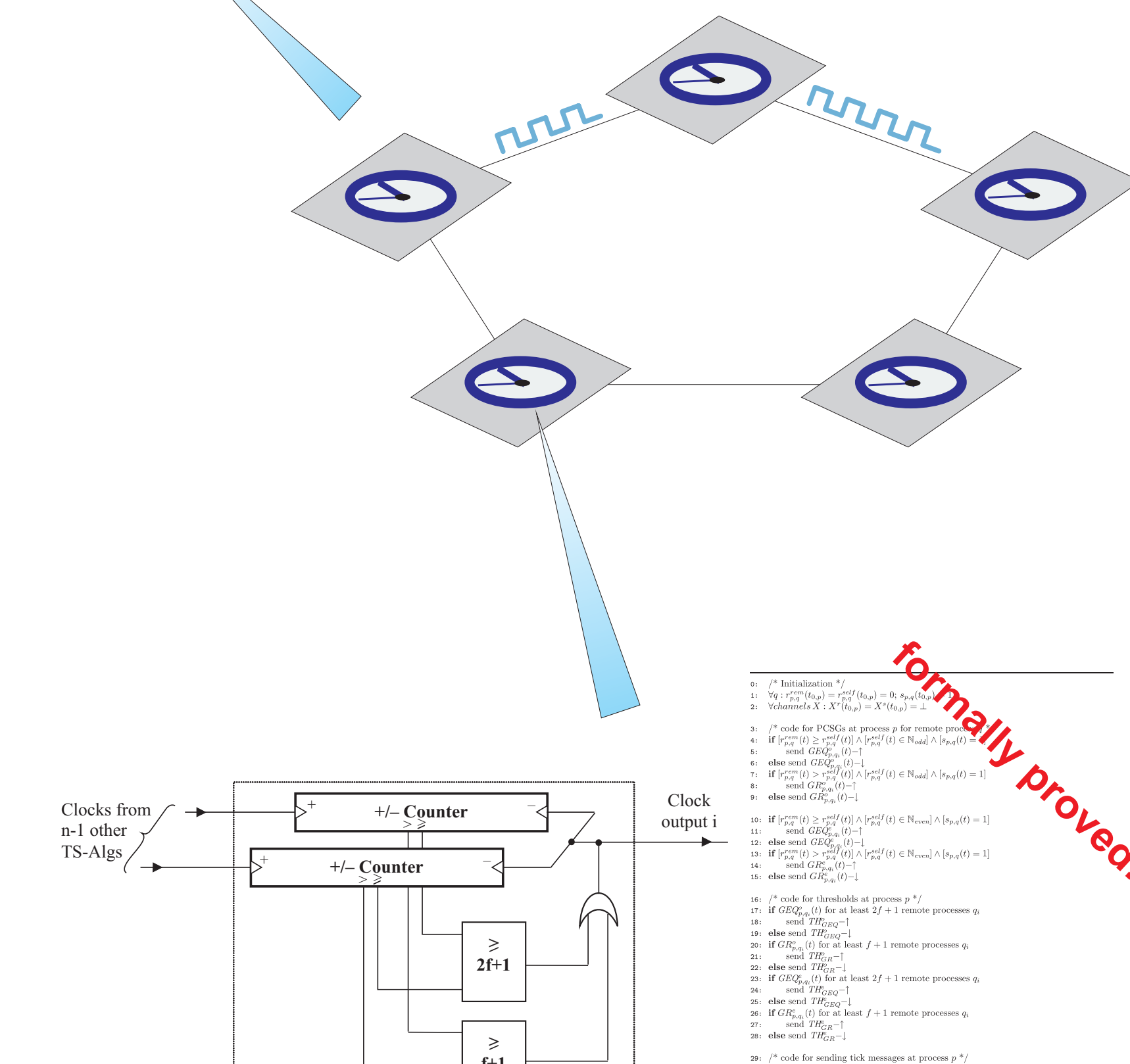
→ Global notion of time!

Graceful Degradation

The clock signals transparently adapt to temperature, physical layout ... of the chip. By contrast, synchronous designs fail if improper overclocking occurs.

Reduced EM Radiation & Ground Bouncing

Local clock signals are not perfectly synchronized, which circumvents simultaneous switching at the entire chip.



DARTS: From fault-tolerant distributed algorithms to space applications. A cooperation between Vienna University of Technology and Austrian Aerospace.

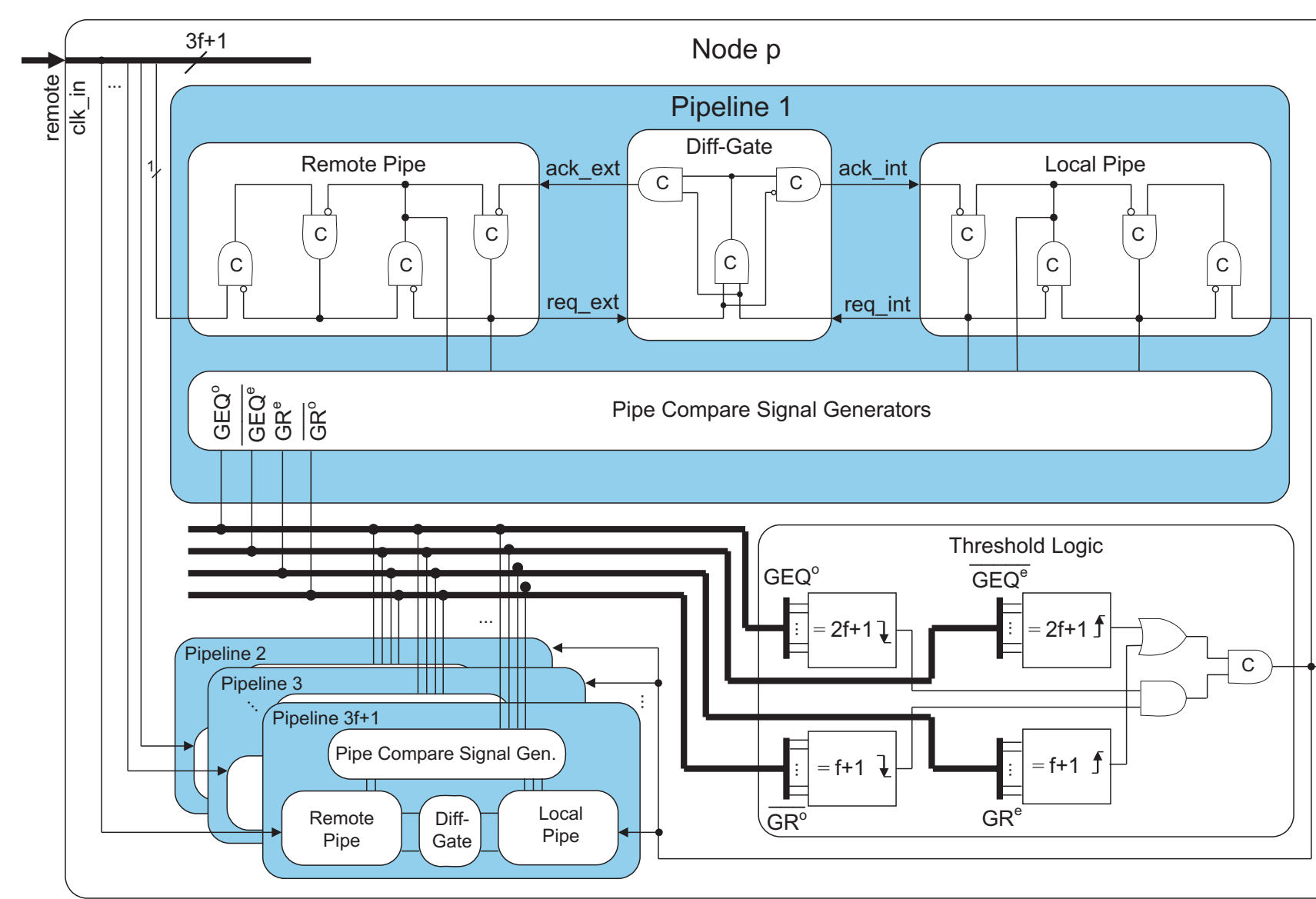
Conclusions:

Achievements:

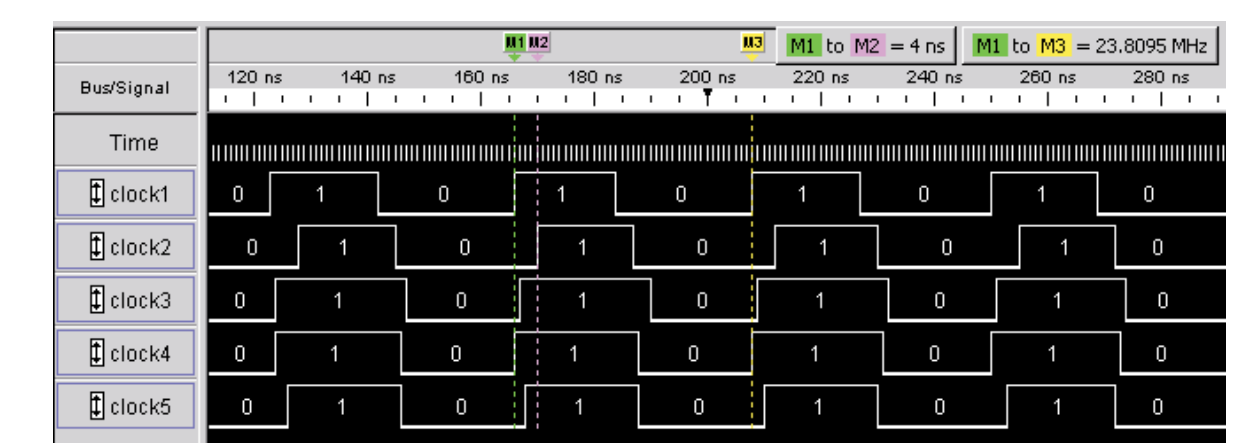
(1) A fault-tolerant clock synchronization algorithm [4] was adapted to obtain a fault-tolerant clock generation algorithm (TS-Alg) that can directly be implemented in hardware.

(2) In the master's thesis it was formally proved that the adapted TS-Alg is correct and provides the required synchronization properties.

(3) The feasibility of a hardware implementation of our TS-Algs was demonstrated by means of an FPGA implementation. Currently we are working on an ASIC implementation.



Hardware implementation of a single TS-Alg.



Signal trace captured by a logic analyzer, showing the clock outputs of 5 TS-Alg units running on an FPGA.

DARTS Literature:

[1] DARTS homepage. <http://www.ecs.tuwien.ac.at/projects/DARTS>
 [2] M. Függer, U. Schmid, G. Fuchs and G. Kempf. Fault-Tolerant Distributed Clock Generation in VLSI Systems-on-Chip. Research Report 12/2006, Technische Universität Wien, Institut für Technische Informatik, 2006
 [3] U. Schmid and A. Steininger. Dezentrale Fehlertolerante Taktgenerierung in VLSI Chips. Research Report 69/2004. (Österr. Patentanmeldung A 1223/2004). Institut für Technische Informatik, 2004
 [4] T.K. Srikanth and S. Toueg. Optimal clock synchronization. Journal of the ACM, 34(3):626-645, July 1987

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