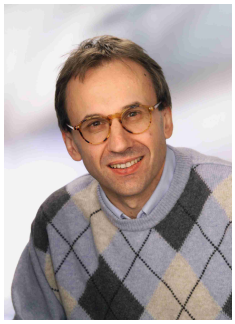
Curriculum Vitae

Ulrich Schmid

April 7, 2018



Personal data:

Surname	Schmid
First name	Ulrich
Title	Univ.Prof. Dr.techn. Dipl.Ing.
Email, Homepage	s@ecs.tuwien.ac.at, http://ti.tuwien.ac.at/ecs/people/schmid
Birth	February 22, 1960 in Randegg (Lower Austria)
Citizenship	Austrian
Religion	Roman catholic
Family status	Married to Dr. Isolde Schmid-Reiter, Ass. Prof. at University of Vienna & Secretary General of European Academy of Music Theatre
Private interests	Music (organist), philosophy, literature, athletics

Education:

1974–1979	Höhere Technische Lehranstalt St. Pölten (Communications Technology and Electronics)
	1979 Matura (with distinction)
1979–1980	Army service
1981–1986	Studies at TU-Wien (Computer Science, Mathematics)
	1985 Diploma Computer Science (with distincion)
	1986 Dr. techn. (with distincion)

Professional activities:

1980–1981	Industrial electronics with company Ing. Steiner, Vienna
1982–1987	Own business (embedded systems)
1987–1988	Research Assistant at Department of Algebra und Discrete Mathematics, TU-Wien
1988–1995	Assistant professor at Department of Automation, TU-Wien
	1995 Habilitation for the entire field of “Informatik”
1995–2003	Associate professor at TU-Wien, Department of Automation
2010	Teaching at Institute of Science and Technology, Austria
2003–now	Full professor for Embedded Computing Systems, TU-Wien

Own Publications

Year	Journal papers
2018	[1, 2]
2017	[3]
2016	[4, 5]
2015	[6, 7]
2014	[8, 9, 10, 11]
2013	[12, 13]
2012	[14, 15]
2011	[16, 17]
2010	[18]
2009	[19, 20, 21]
2008	
2007	[22]
2006	[23]
2005	
2004	[24]
2003	
2002	
2001	[25]
2000	
1999	[26, 27]
1998	
1997	[28, 29, 30]
1996	[31]
1995	[32]
1994	[33, 34, 35, 36, 37, 38]
1993	
1992	[39]
1991	[40, 41]
1990	[42, 43]
1989	[44, 45, 46]
1988	[47]
1987	[48]
1983	[49]

Year	Conference papers
2018	[50, 51]
2017	
2016	[52, 53]
2015	[54, 55, 56]
2014	[57, 58, 59]
2013	[60, 61, 62, 63, 64, 65, 66, 67, 68]
2012	[69, 70]
2011	[71, 72, 73, 74, 75]
2010	[76, 77, 78, 79, 80]
2009	[81, 82, 83, 84]
2008	[85, 86, 87, 88, 89]
2007	[90, 91]
2006	[92, 93, 94, 95, 96, 97]
2005	[98, 99, 100, 101]
2004	[102]
2003	
2002	[103, 104, 105]
2001	[106, 107]
2000	[108, 109, 110, 111, 112]
1999	[113, 114]
1998	[115, 116, 117, 118]
1997	[119]
1996	[120, 121, 122]
1995	[123]
1994	[124, 125]
1993	[126, 127, 128]
1992	[129, 130, 131, 132]
1991	[133, 134]
1990	
1989	
1988	
1987	
1983	

Year	Books
2009	
1996	
1990	[135]

	Editorials
2009	[136]
1996	[137]
1990	

Year	Technical Reports
2018	
2017	[138, 139]
2016	[140, 141]
2015	[142, 143]
2014	[144, 145, 146, 147]
2013	[148, 149]
2012	[150, 151, 152]
2011	
2010	[153, 154]
2009	[155, 156, 157]
2008	[158, 159]
2007	[160, 161, 162, 163]
2006	[164, 165, 166, 167, 168]
2005	
2004	[169, 170, 171, 172, 173, 174, 175, 176]
2003	[177, 178, 179, 180, 181, 182]
2002	[183, 184]
2001	[185, 186, 187, 188, 189, 190, 191]
2000	[192, 193, 194, 195, 196]
1999	[197, 198, 199, 200, 201, 202]
1998	[203, 204, 205, 206]
1997	[207, 208]
1996	[209, 210, 211]
1995	[212, 213, 214]
1994	[215]
1993	[216, 217, 218, 219]
1992	[220, 221]
1991	[222, 223, 224, 225, 226]
1986	
1985	

Year	Other publications
2018	
2017	
2016	[227]
2015	[228]
2014	[229]
2013	[230]
2012	[231, 232, 233, 234, 235, 236]
2011	
2010	
2009	
2008	
2007	
2006	[237]
2005	[238]
2004	
2003	
2002	[239]
2001	[240]
2000	
1999	
1998	
1997	[241, 242]
1996	[243]
1995	
1994	[244]
1993	[245]
1992	
1991	
1986	[246]
1985	[247]

Statistics

Art	#	#best	#invit.	$\sum p.$	Avg.$p.$	Min.$p.$	Max.$p.$
Journals	49		6	1133	23	3	75
Conferences	84	4	6	732	9	1	26
Books	1			400	400	400	400
Editorials	2			420	210	60	360
Technical Reports	89			3469	39	3	400
Others	21			352	17	1	132
Sum:	**246**	**4**	**12**	**6506**			

Supervision

Year	Dissertations
2014	[248]
2013	
2012	
2011	[249]
2010	[250]
2009	[251, 252]
2008	
2007	
2006	[253]
2005	[254, 255]
2004	[256, 257]
2003	
2002	[258]
2001	
2000	
1999	[259]
1998	[260]
1997	
1996	[261]
1995	
1994	[262]
1993	
1992	
1991	

Year	Masters/Diplomas
2014	
2013	[263, 264, 265, 266]
2012	[267]
2011	
2010	[268, 269]
2009	
2008	
2007	
2006	[270]
2005	[271]
2004	[272]
2003	
2002	[273, 274, 275]
2001	
2000	[276, 277]
1999	[278]
1998	
1997	[279, 280]
1996	[281, 282]
1995	[283]
1994	[284, 285, 286, 287]
1993	
1992	[288]
1991	[289]

Some Highlights ...

Research

- (Co-)Author of 130+ journal and conference publications; supervisor of 100++ publications of group members
- Austrian START prize (1996), Kardinal Innitzer Förderungspreis (1995)
- Several best papers [87, 70], invited papers [17, 26] and keynotes [85, 290]
- Some patents [171, 193]
- Selected accomplishments:
  - Models for fault-tolerant distributed algorithms in VLSI circuits [4, 54, 9, 13, 14]
  - Agreement in distributed systems with process and link failures [1, 52, 291, 19, 16, 103]
  - Partially synchronous system models [20, 98, 21, 291, 17]
  - Interval-based clock synchronization [27, 32, 26]
  - Distributed computing models for real-time systems [10, 89]
  - Automatic competitive analysis of real-time systems [2]
  - Analytic combinatorics in queueing systems analysis [41, 36]
- PC-chair DISC'18, PC-member in many scientific conferences (PODC, DISC, OPODIS, ICDCS, IPDPS, EDCC, SSS, etc.)

Teaching

- Supervisor of 10+ PhD and 25+ Master theses
- Rich experience in design and teaching of courses in the areas fault-tolerant distributed algorithms and real-time systems
- Co-author of textbook *Informatik* (Springer, 3 editions) [135]

Management and Administration

- Acquisition of 15+ big research projects, including

Leader	*Title*	*Funding*	*Agency*	*Duration*
U. Schmid	Fault-Tolerant Asynchronous Logic (FATAL)	EUR 451k	FWF/ P21694	2009–2014
R. Bloem	NFN Rigorous Systems Engineering (RiSE+SHiNE)		FWF/	2011–now
	PP05: Reconciling Distributed and Real-Time Computing	EUR 749k	S11405	
U. Schmid	Gracefully Degrading Agreement in Directed Dynamic Networks (ADynNet)	EUR 350k	FWF/ P28182	2016–now
G. Gottlob	Doctoral College LogiCS		FWF/	2018–now
	Full faculty member (2 PhDs)	EUR 350k	W1255	

- Designer and coordinator of Bachelor and Master curriculum "Computer Engineering"
- Designer and program coordinator "Bachelor with Honors"
- Coordinator of major research focus "Technische Informatik"
- Speaker of the full professors of the faculty; member of many faculty boards

Detailed Information ...

Research

Brief description of the primary goals in scientific research:

- Knowledge-driven scientific investigation of relevant and difficult problems in all areas of computer engineering.
- Quality before quantity.
- Creation of an optimal research climate based upon freedom and achievement motivation.
- Primary focus on leading own (TU Wien) students towards internationally competitive research.
- Setup of cooperations with competent—and, if possible, locally available—experts in all project-relevant disciplines.
- Support for activities demonstrating the relevance of the pursued research, e.g., by stimulating/supporting projects that transform our scientific results into prototypes or even industrial pilot applications.

Prices, Awards and Invitations

- START prize of the Ministry of Science and Research (1996, see [209, 241, 192, 240]), the most prestigeous award for young scientists in Austria; EUR 1.000.000,– freely available research funding for 6 years.
- Kardinal Innitzer-Förderungspreis (1995) for the accomplishments of the "Habilitationsschrift" [36].
- Best papers: IFAC WRTP'94 [128], WRTP'99 [116], SSS'08 [87], DSD'12 [70].
- Invited keynotes and tutorials: IFAC WRTP'2000 [109], ISPCS'07 [290], SSS'08 [85], FORMATS'10 [79], DARS'16 [292]
- Invited panels and seminars: Panel COMPSAC'98 [117], several Dagstuhl seminars [245, 243, 242, 293, 227]
- Invited Papers: Control Engineering Practice [25, 33], J. Real-Time Systems [26], e&i [24, 23], Theoretical Computer Science [17], Microprocessors and Microsystems [13].

Supervised PhD Thesises

1. Alexander Kößler. Real-Time Performance Analysis of Synchronous Distributed Systems. 2014.
2. Peter Robinson. Weak System Models for Fault-Tolerant Distributed Agreement Problems. 2009.
3. Matthias Függer. Analysis of On-Chip Fault-Tolerant Distributed Algorithms. 2010.
4. Martin Biely. Dynamic Aspects of Modeling Distributed Computations. 2009.
5. Heinrich Moser. A Model for Distributed Computing in Real-Time Systems. 2009 (summa cum laude; Promotion "sub auspiciis praesidentis").
6. Hannes Stratil. Advantages and Limitations of Position-based Communication in Wireless Ad-hoc Networks. 2006.
7. Martin Hutle. Failure Detection in Sparse Networks. 2005.
8. Bernd Thallner. Topology Control for Fault-Tolerant Communication in Wireless Ad Hoc Networks. 2005.
9. Josef Widder. Distributed Computing in the Presence of Bounded Asynchrony. 2004.
10. Bettina Weiss. Authenticated Consensus. 2002.
11. Klaus Schossmaier. Interval-based Clock State and Rate Synchronization. 1998.
12. Dietmar Loy. GPS-Linked High Accuracy NTP Time Processor for Distributed Fault-Tolerant Real-Time Systems. 1996.
13. Stefan Stöckler. Event-based monitoring of distributed real-time systems. 1994.

PhD co-supervisor:

1. Samar Khattab. Efficient Interference Reduction in Low Complex Digital Direct Sequence Spread Spectrum Systems. Faculty of Electrical Engineering and Information Technology, TU-Vienna, 2010.

External PhD thesis committee member:

1. Andreas Pavlogiannis (IST Austria)
2. Thomas Nowak (Ecole Polytechnique Paris)

Activities in the Scientific Community

- PC chair DISC'18
- Chair of PODC'18/DISC'18 Dijkstra Prize award committee
- General chair DISC'17, October 2017, Vienna (with J. Widder)
- Organizer Dagstuhl-Seminar 08371 "Fault-Tolerant Distributed Algorithms in VLSI Chips" (with Jo Ebergen, Bernadette Charron-Bost und Shlomi Dolev) [293], Dagstuhl castle, Germany, September 2008.
- Associate Editor for Journal of Scheduling (until 2004), J. Real-Time Systems (until 2010).
- Program committee member of WRTP'00, DSN'01, DISC'01, WRTP'03, SenSys'04, WRTP'04, OPODIS'05, DIWANS'06, OPODIS'06, PODC'07, SSS'08, IPDPS'09, EDCC'10,ICDCS'10,WRAS'10,IPDPS'10,ICDCS'11, ICDCS'11, LAFT'11, EDCC'11, SSS'12, ICDCN'12, EDCC'12, SIROCCO'13, EDCC'14, SOFSEM'15, DISC'15, ICDCN'16, CERTS'16, PODC'18
- Research management policies:
- Member in steering committee of the BM:vit research funding (programme FIT-IT "Embedded Systems", until 2012).
- Project reviews for National Science Foundation, IRISA, Israel Science Foundation.
- Tenure reviews for TU-Wien, UCSD, EPFL, Ecole Polytechnique Paris, INRIA, Technion Haifa.
- Paper reviews for international journals and conferences: Algorithmica, ICALP, Information and Computation, ISADS, J. Algorithms, Real-Time Systems, Software Practice & Experience, The Computer Journal, Theoretical Computer Science, IEEE Transactions on Parallel and Distributed Systems, IEEE Transactions on Networks, J. Scheduling, J. Systems Architectures, IEEE Transactions on Computers, ACM Computing Surveys, IEEE Transactions on Software Engineering, Distributed Computing, SIAM J. Computing, Journal of Applied Logic, J. of Circuits, Systems, and Computers, J. Software Testing and Verification; WRTP, DISC, DSN, CCN, PODC, IFAC World Congress, OPODIS, SenSys, DIWANS, SSS, IPDPS, EDCC, ICDCS, SIROCCO, WRAS, LAFT, ICDCN, STOC, SOFSEM, CERTS.

Memberships

Overview Research Projecs

- Project **Rigorous Systems Engineering** (RiSE+SHiNE, *http://arise.or.at*), see [61, 62, 63, 67, 68, 59, 229, 6, 292, 227, 2, 50] and [294, 295, 248]. Supported by Austrian Science Fund (FWF) National Research Network (NFN) S11405 [Project part PP05: Reconciling Distributed and Real-Time Computing], in collaboration with H. Veith (TU Wien), K. Chatterjee (IST Austria) and E. Bartocci (TU Wien, sub-task leader PP05 SHiNE).

  Devoted to the application of formal verification methods to problems in distributed computing and real-time computing. Core results are a method for parameterized model checking of fault-tolerant distributed algorithms [67] and applying algorithmic game theory for competitive analysis of real-time scheduling algorithms [2].

- Project **Fault-tolerant Asynchronous Digital Circuits**, see [158, 156, 81, 76, 71, 14, 70, 15, 231, 232, 233, 234, 235, 236, 12, 13, 60, 64, 65, 66, 230, 57, 8, 9, 144, 54, 55, 7, 228, 4, 5, 3] and [296, 250, 297, 267, 265, 266]. Supported by the Austrian Science Fund (FWF) project P21694 [Fault-tolerant Asynchronous Logic (FATAL) *http://ti.tuwien.ac.at/ecs/research/projects/fatal*], a collaboration with the Institute of Electrodynamics, Microwave and Circuit Engineering and the Institute of Atomic and Subatomic Physics at TU-Wien. International collaborations with D. Dolev (Hebrew University Jerusalem) and C. Lenzen (MPI Saarbrücken), Kay-Obbe Voss (GSI Darmstadt) and Ulrich Giesen (PTB Braunschweig), and by the FWF projekt P26436 [Self-stabilizing Byzantine Fault-Tolerant Distributed Algorithms for Integrated Circuits (SIC) *http://ti.tuwien.ac.at/ecs/research/projects/sic*].

  Development of the mathematical/formal foundations of a framework for the hierarchical modeling and analysis of fault-tolerant asynchronous VLSI circuits, using fault-tolerant distributed algorithms knowledge in conjunction with the experimental assessment of both radiation-induced failures and metastability in modern VLSI technology. Core results are a suitable computing and system model [14], including an extension to self-stabilizing algorithms [9], digital [13, 3] and analog [15] modeling of single-event transients, and digital modeling of glitch-propagation and metastability [4, 55, 51]. Applications: Self-stabilizing Byzantine fault-tolerant clock generation [8, 9] and clock distribution [5] in SoCs.

  Publications appeared in first-rate journals und conference proceedings; best paper award [70], invited paper [13].

- Project **Partially synchronous models for distributed systems**, see [179, 177, 178, 182, 169, 102, 98, 99, 101, 95, 165, 96, 20, 21, 86, 87, 17, 89, 159, 84, 157, 83, 72, 73, 149, 10, 11] and [298, 299, 300, 301, 255, 302, 303, 304, 305, 251, 252, 249]. Supported by the FWF projects P17757 [Asynchronous Distributed Algorithms in the Θ-Model (Theta), *http://ti.tuwien.ac.at/ecs/research/projects/theta*], P20529 [Partially Synchronous Distributed Real-Time Systems (PSRTS), *http://ti.tuwien.ac.at/ecs/research/projects/psrts*)] and the FIT-IT "Embedded Systems" PhD stipend 808198 [Distributed Computing in the Presence of Bounded Asynchrony (DCBA)]. International collaborations e.g. with G. LeLann (INRIA Rocquencourt), Ch. Fetzer (TU Dresden) and D. Malkhi (Microsoft Research).

  Definition and investigation of novel partially synchronous system model, which allows the definition of asynchronous algorithms for fault-tolerant distributed real-time systems. Core results are the Θ-Model [101], the FAR model [98], the WTL model [21, 84] and the ABC model [17]; focus on k-set agreement [84, 73]. Real-time scheduling analysis is suppoted by the real-time distributed computing model [95, 303]. Promising applicability in the area of VLSI Systems-on-Chip [14, 76].

  Publications appeared in first-rate journals and conference proceedings; best Paper Award [87], invited paper [17], keynote [85] and tutorial [79].

- Project **Distributed Algorithms for Robust Tick-Synchronization** (DARTS, *http://ti.tuwien.ac.at/ecs/research/projects/darts*), see [172, 171, 93, 97, 92, 164, 166, 163, 90, 23, 88, 85, 136, 82, 81, 76, 14] and [306, 270, 307, 296, 250, 268, 308]. Joint project with Austrian Aerospace (now Ruag Austrian Aerospace). Supported by the award-winning FIT-IT "Embedded Systems" project 809456 (DARTS).

  Application of asynchronous fault-tolerant Θ-algorithms in VLSI systems-on-chip. Central results are mathematical correctness proofs and performance analyses [14, 76] as well as a complete ASIC implementation [308].

  International patent application [171] and invited paper [23]. Organization of a Dagstuhl seminar [136] and invited keynote [85] at SSS'08.

- Project **Fault-tolerant Distributed Algorithms in Dynamic Networks**, see [34, 214, 200, 192, 111, 196, 190, 106, 186, 185, 107, 191, 184, 183, 103, 309, 181, 176, 175, 174, 170, 173, 310, 311, 94, 22, 18, 21, 19, 312, 78, 77, 74, 69, 58, 56, 52, 227, 53, 1] and [313, 314, 315, 316, 317, 318, 319, 320, 258, 273, 274, 321, 322, 323, 324, 325, 326, 327, 328, 329, 330, 331, 332, 333, 334, 335, 330, 271, 254, 255, 253, 336, 337, 237, 338, 339, 304, 252, 263, 264]. Supported by the Austrian START price Y41-MAT [project W2F *http://www.ecs.tuwien.ac.at/projects/W2F/*] and the FWF projekts P18264 [Fault-Tolerant Distributed Algorithms in Sparse Ad Hoc Wireless Networks (SPAWN), *http://ti.tuwien.ac.at/ecs/research/projects/spawn*] and P28182 [Gracefully Degrading Agreement in Directed Dynamic Networks (ADynNet) *http://ti.tuwien.ac.at/ecs/research/projects/adynnet*]. International collaborations with I. Keidar (Technion Haifa), D. Malkhi (Microsoft Research), A. Schiper (EPFL), B. Charron-Bost (Ecole Polytechnique Paris), T. Nowak (ENS Paris), M. Biely (EPFF) and P. Robinson (NSU Singapur).

  Development of the theoretical and algorithmic foundations for fault-tolerant distributed real-time systems based on incomplete and/or highly time-varying communication topologies, e.g., wireless ad-hoc networks. Major achievements comprise a hybrid failure model for process and link failures, fault-tolerant communication and Voronoi-aided routing, algorithms for system booting, and failure detectors for sparse communication graphs. Systematic exploration of agreement (consensus, k-set agreement etc.) in directed dynamic networks [1, 52].

- Project **Synchronized Universal Time Coordinated for Distributed Real-Time Systems** (SynUTC, *http://www.ecs.tuwien.ac.at/SynUTC/*), see [33, 32, 31, 28, 29, 26, 27, 128, 122, 119, 115, 116, 113, 114, 108, 110, 196, 216, 215, 212, 243, 211, 207, 208, 242, 30, 204, 118, 197, 198, 199, 201, 192, 193, 187, 104, 105], [137, 290] and [287, 283, 340, 341, 261, 281, 342, 343, 344, 279, 280, 345, 346, 347, 348, 260, 349, 278, 350, 351, 352, 353, 354, 256]. Supported by the Austrian Science Fund under grant P10244-ÖMA, the Austrian START-Programme Y41-MAT, the Austrian Ministry of Science under contract Zl.601.577/2-IV/B/9/96, and the Austrian National Bank (OeNB) under grant 6454. Joint project with the Department of Computer Technology (TU-Wien) and the Department of General Electrical Engineering and Electronics (TU-Wien).

  Development of theoretical foundations and hardware+software for providing a highly accurate global time in distributed fault-tolerant real-time systems. Interval-based approach, utilizing an integration of clock synchronization and GPS satellite receivers. Major achievements e.g. an elaborate hardware support (UTCSU-ASIC), novel clock synchronization algorithms, a powerful simulation framework, and a comprehensive mathematical/formal and experimental analysis. Best papers at IFAC WRTP'94 [128] und WRTP'99 [116], best student paper DSN'01 [353]; solution to the more than 10-year-old problem of finding a fault-tolerant intersection function satisfying a Lipschitz condition (L. Lamport) [27].

  Papers published in first-rate international journals and conference proceedings. Many invited papers and talks [33, 26, 113, 108, 109, 243, 242]; presentation at the "Hannover Messe'98" [204]; Patents [208, 193]

and industrial pilot applications. Further exploitation of results by spin-off company *Oregano Systems* in the context of FIT-IT projec PSynUTC. Keynote speech at ISPCS'07 [290].

- Project **Versatile Timing Analyzer** (VTA) for monitoring of distributed real-time systems, see [39, 133, 129, 130, 131, 127, 124, 225, 220, 217] and [355, 356, 357, 358, 359]. Supported by the Austrian Science Fund under grant P8390-TEC.

  Foundations and Development of a general-purpose monitoring systems for timing analysis in distributed real-time systems. Major achievements e.g. maximum target-system independent, runtime code-instumentation, object oriented event definition language with formal semantics, and distributed event recognition and processing.
- Project **Performance Models and Load Assumptions for Scheduling in Soft Real-Time Systems** (topic of Habilitationsschrift), see [45, 46, 42, 43, 40, 35, 36, 245, 222, 210].

  Mathematical/theoretical quantification of *deadline meeting capabilities* of scheduling algorithms for probabilistic aperiodic tasks in real-time systems. Utilization of advanced combinatorial and asymptotic methods allows a respective performance analysis without stable state assumptions.

  Papers—including Habilitationsschrift—published in first-rate international journals; presentation at Dagstuhl-Seminar "Average Case Analysis of Algorithms".
- Project **Broadcast Random-Access Communications in Computer Networks, Models and Analysis** (Department of Algebra und Discrete Mathematics), see [48, 47, 44, 41, 134, 246, 223, 221]. Supported by the Austrian Science Fund (FWF) under grant P6477P.

  Mathematical/theoretical investigation of characteristic parameters (primarily throughput and stability) of protocols for multiple access broadcast networks à la Ethernet. Results are e.g. the solution of the 20-year-old problem of the *time-to-instability* of ALOHA networks and a thorough investigation of the impact of *channel capture*.

Development activities

Development Activities in Research Projects

Software and hardware development of systems supporting research projects or transforming research results into prototype systems:

- General outline of the *Primitive Event Management* (target interface, external event recognition) of our *Versatile Timing Analyzer* VTA.
- Object-orientiented design of the VTA software (CRC-Cards) and basic considerations concerning the human interface, in particular data analysis and visualization.
- Design of our *Distributed Object-Based Operating Systems* DOBOS built on top of SunOS and pSOS$^{+\mathrm{m}}$ to be used for the VTA, see [123, 120, 218].
- Hardware architecture of a 802.3DCR LAN coprozessor for a Force M68030 VMEbus CPU-30 (for projects VTA und SynUTC).
- Planning of measuring equipment for experimental long-term evaluation of GPS satellite receivers (for project SynUTC), see [119].
- Specification and architecture of the Network Time Interface (NTI) M-Module (for Project SynUTC), see [211, 198].
- Concept of a high-performance device driver for the abovementioned LAN coprocessor, for integration in a pSOS^{+m} multiprocessor system.
- Low-level programming of the NTI and HW/SW debugging of AcQ i6360 and MEN A203 M-Module carrier boards, see [197].
- Redesign, test and evaluation of the NTI Device-Driver + NTI on Motorola's MVME-162 CPU under pSOS^{+m}, see [199].
- Specification and setup GPS Device-Driver for the NTI, see [201].
- Setup of a pSOS^{+m} development environment for MVME-162 CPUs.
- Development of an embedded clocksynchronization demo application for SynUTC, see [114].
- Installation und Setup Lauterbach-Debugger for PowerPC MPC555- and M68040-Targets under Enea OSE.
- Collaborative work on specification of professional implementation of SynUTC software and hardware (FIT-IT project PSynUTC by spin-off company Oregano Systems) [187].
- Development of a SynUTC-synchronized networked embedded system using MPC555 und MPC860 CPUs under OSE [277].
- Definition, coordination and participation in building up HW and SW of FIDIS cluster (20 Ethernet+CAN-coupled MEN EM1N PowerPC microcontrollers, QNX Neutrino RTOS, Lauterbach development tools)

Development Projects with own Business (1982–1991)

Development projects in the area of microprocessor systems and industrial electronics:

- Development of a second generation *Informator*-system (for Tirolean tourist agency).
- Development of a multitasking operating system kernel (SMX-65) for 6502 microprocessors.
- Development of a high-level macro language for assembler programming, see [49].
- Development and production of a programmable controlling system for oil-fueled heating installations.
- Development and production of a teaching aid for courses on aural training for students in music (Musikakademie Graz).
- Development of a multiuser telex system for office automation (sold by company Ph. Liebisch, Vienna).

Industrial Employment with Company Ing. Steiner, Vienna (1980–1981)

Work on development projects in the area of microprocessor systems and industrial electronics:

- In-circuit emulator for microprocessor 6502.
- Bus-coupler *Commodore Bus* to *Steiner "Puzzle"-Bus*.
- Miscellaneous (production-)test software, e.g. for parallel I/O board and floppy controller.
- Data aquisition system for automated book printing (for the Austrian publisher *Überreuter*).
- Remote accommodation service system *Informator* (pilot project for the tourist office Kitzbühel).

Patents

Patents (applied personally or via firms) on results of own research.

1. Baur Prüf- und Meßtechnik (A-6832 Sulz, Austria): *Energiekabel-Fehlerortung*, see [208]
2. Nikolaus Kerö, Ulrich Schmid, Martin Horauer: *Uhrensynchronisation in Netzwerken*, see [193]
3. Ulrich Schmid, Andreas Steininger: *Dezentrale Fehlertolerante Taktgenerierung in VLSI Chips*, see [171]

Teaching

Own courses

Verteilte Algorithmen (2004-now)

6 ECTS mandatory lecture + practical in Master curriculum "Technische Informatik", based on the book *Distributed Algorithms* by H. Attiya und J. Welch.

Seminars

- 3 ECTS mandatory seminar **Scientific Working** in Bachelor curriculum "Technische Informatik" (2011–now). Introduction to scientific working and scientific communities; literature search; writing, reviewing and presentation of a scientific paper.
- 3 ECTS mandatory seminar **PhD Primary Area Computer Engineering Introduction** for Vienna PhD School of Informatics (2009–2013, jointly with A. Steininger).
- 3 ECTS optional research seminar **Rigorous Systems Engineering** (TU Wien and IST Austria)
- 3 ECTS Pflichtproseminar **Wissenschaftliches Arbeiten** (1992–2006).

Real-Time Scheduling (2005-now)

3 ECTS optional lecture + practical in Master curriculum "Technische Informatik", based upon the book *Deadline Scheduling for Real-Time Systems* by J. Stankovic, M. Spuri, K. Ramamritham and G. Buttazzo.

Building Reliable Distributed Systems (2011-now)

4.5 ECTS optional practical in Master curriculum "Technische Informatik" (jointly with M. Függer and A. Kößler). Implementation of simple distributed algorithms on microcontroller boards running a real-time operating system (QNX, VxWorks, RTLinux).

Problems in Distributed Computing (2011-now)

3 ECTS optional lecture + practical in Master curriculum "Technische Informatik". Introduction of advanced topics in distributed algorithms; joint reading and student's presentations of selected scientific papers.

Supervision

Supervision of practical [38] and scientific projects, Bachelor theses, Master/Diploma theses and dissertations.

Advanced Distributed Algorithms (IST Austria, 2009)

Three hours lecture + practical am Institute of Science and Technology (IST) Austria, for PhD Students der PhD School of Informatics an der TU-Wien und der PhD School am IST Austria.

Distributed Algorithms for Fault-Tolerant Real-Time Systems (2007-2010)

Two hours optional lecture + practical devoted to real-time scheduling in networked distributed systems.

Ausgewählte Kapitel der Technischen Informatik X (1998–2006)

Two two-hours lecture + practical devoted to distributed algorithms for introducing interested students to our research projects. Individual work + presentation of the solution of a scientific problem.

Lecture + Practical "Modellierung, Design und Analyse von Echtzeitsystemen" (1992–2002)

2+2-hour special course (lecture+practical) for students of *Technical Computer Science*, devoted to an introduction into the industrial state-of-the-art in embedded systems' design. Utilizes hardware/software environment of the practical "Prozeßautomatisierung".

Practical "Prozeßautomatisierung" (1989–1992)

Basic course in computerized automation for all students of computer science.

- **1989–1992:** Definition of content, implementation and running the course for about 300 participants/year, see [224], [126].
- **1993–2000:** Design of a new course devoted to embedded systems in computerized automation. Major responsibility for contents, implementation and running the practical for about 200 participants/year, see [125, 121, 37, 194].
- **2000–2002:** Design of a new 1,5 hours/week process-control-oriented basic course on computerized automation. Major responsibility for concept, contents and organization of the practical for about 200 participants/year.

Lecture "Einführung in die Informatik I" (1989–1992)

Introductional course in computer science (Prof. G.-H. Schildt). "Architect" and co-autor of the text-book *Informatik*, see [135].

Other Activities Related to Teaching

FIT-IT Projekt Seamless Campus - Distance Labs (SC-DL)

BM:VIT FIT-IT Embedded Systems accompanying measures project (SC-DL, *http://ti.tuwien.ac.at/ecs/research/projects/scdl*), devoted to the development of a distance learning concept for the labs Microcontroller (carry-out equipment) and Digital Design (remote workplaces), including a web portal for the whole "Technische Informatik" at TU-Wien [360, 361].

Bachelor with Honors Program

Design of the general structure, detailed planning and implementation of a Bachelor with Honors program according to anglo-american standards: BHons "emulates" a 4-year Bachelor, by means of individually selected additional courses (45-60 ECTS). Solely performance-based admission and graduation criteria, individual mentoring.

- Design structure and criteria

- Implementation BHons as official program of TU Wien, in all Bachelor programs in Informatik
- Setup internship exchange program
- Aquisition scholarships

Miscellaneous

- Course evaluations and quality assessment
- Presentation Bachelor curriculum "Technische Informatik" (Beginner's Day, Info Day, etc.)
- Student selection and comprehensive exam in primary area "Computer Engineering" in PhD School of Informatics of TU Wien (until 2012)
- Mentoring BHons students

Administration

Activities at the Institut für Technische Informatik/Embedded Computing Systems Group (2003–now)

- Founded by appointing me professor and head of the former VLSI-Design Group in 2003:
  - Development and dissemination of mission, goals and strategy of the new ECS group
  - Identifying joint research work
  - Planning of renovation and new furniture
  - Supervision of planning a chipcard-based access control and video surveillance system of ECS group + Informatik-Labor Treitlstraße
  - Financing scheme and budgets negotiation
- Global activities related to the institute
  - Development of institute's organization guidelines
  - Planning and supervision/coordination of maintenance and extension of the TI Web-Portal
  - Content provision for TI Web-Portal
- Integration of Computer Architecture professor (M. Shafique)

Activities at the Department of Automation (1988-2003)

- Building up the department's infrastructure (when Prof. G.-H. Schildt was appointed to the departments head in 1988):
  - Planning and purchase of the workstation network and other equipment: HP/Apollo-Workstations, peripherals, software
  - UNIX system management, see [226]
- Management of Department's funds, including planning and purchase of new equipment
- Planning of extension/rebuilding of the department
- Writing the department's activity reports

Membership in faculty committees

- Gerätekommission der Fachgruppe Informatik (1988–now)
- Institutskonferenz (1988–1991)
- Fakultätskollegium (1990–1994)
- Kommission zur Vergabe von Leistungs- und Förderungsstipendien der Fakultät (1992–1999)
- Budget- und Stellenplankommission der Fakultät (1995–1999)
- Raumplanungskommission der Fakultät (1995–1999, 2007)
- Fakultätsrat (2004–now)
- Studienkommission Informatik (2004-now)
- Advisory-Board of the Dean (2011–now)

- Jury Epilog (Master thesis award), Siemens PhD-Stipend
- Berufungskommission "Interaktive Systeme", "Embedded Systems" (Faculty of Electrical Engineering), "Algorithmen und Datenstrukturen", "Security", "Computer-Aided Verification", "Parallel Computing", "Dependable Systems", "Systems-on-Chip" (Fakult"at Elektrotechnik), "Security", "Ubiquitous Computing", "Computer Architecture"
- Candidate reviews for professorship "Diskrete Mathematik" (Fakultät Mathematik)
- Habilitationskommissionen
- Directing committee member PhD-School of Informatics (until 2012)
- Speaker of the faculties Professorenkurie (2016–now)

Structural Concepts for Faculty and TU-Wien

- Development of model for capacity planning and staff disposition for faculty, see [203]
- Development of model for capacity planning and staff disposition for Fachgruppe Informatik, see [203, 205]
- Assessment of teaching load vs. capacity for faculty [202]
- Development of a computer lab organization plan for the faculty, see [206, 188]
- Participation in the definition of the development plans of the faculty [362]
- Coordinator of the major research focus "Technische Informatik"
- Designer and coordinator of the Bakkalaureats- and Magisterstudium "Technische Informatik" (2002–now) [189]
  - Head of working group
  - Initial proposals
  - Coordination with faculty of electrical engineering, mathematics and physics.
  - Coordination with IST Austria
- Development of a course admission control strategy ("Score-Model")
- Development and coordination of a *Bachelor with Honors* program

Creation of Laboratories and Infrastructure

- Building up the Informatik-Labor Treitlstraße 1 (1993–1994), primarily dedicated to the courses *Software-Engineering* (Department of Software Technology) and *Prozeßautomatisierung* (Department of Automation), see [213]. Overall costs approx. 3.2 Mio.ATS.
- Building up the "Informatik-Labor f"ur Prozeßautomatisierung und Embedded Systems" (1999–2000); total cost about 2.1 Mio.ATS.
- Definition, proposal and coordination of Uni-Infrastruktur III projekt "Networked Embedded Systems Research Cluster" (2005-2007); granted funding EUR 488.000,–
- Coordination and planning of renewal of the mandatory labs for Technische Informatik (2005-2006); total costs approx. EUR 350.000,–.
- Definition and proposal for Uni-Infrastruktur IV projekt RES [161] (2007); granted funding approx. EUR 2.050.000,–. Inter-faculty initiative (Informatik, Electrical Engineering, Physics) for establishing a new professorship "Computer-Aided Verification" und infrastructure for experimental evaluation of robust embedded systems.

Research Management

- Project proposal and management FWF-project P6477P (1987–1988, project head: Helmut Prodinger, Department of Algebra und Discrete Mathematics), funding approx. 0.4 Mio.ATS.
- Project proposal and management FWF-Projekt *Versatile Timing Analyzer* (VTA, P8390-TEC, 1991–1995) [225, 217], overall funding approx. 1.9 Mio.ATS.
- Project proposal and management FWF/START-project *Synchronized Universal Time Coordinated for Distributed Real-Time Systems* (SynUTC, P10244-ÖMA, 1995–now) [216, 192], overall funding approx. 6 Mio.ATS. Joint project with Department of Computer Technology (TU Wien) and Institute of General Electrical Engineering and Electronics (TU Wien).
- Project proposal and management FWF/START-project *Sequenced Synchronized Clock Message Protocol/ Wireline/Wireless Factory/Facility Fieldbus* (SSCMP/W2F, 1997–2004) [214, 209, 192], overall funding approx. 7 Mio.ATS.

- Project proposal and management project *Prototypenentwicklung f"ur SynUTC* (BMWV Auftragsforschung GZ. 601.577/2-IV/B/9/96 + OeNB "Jubil"aumsfonds"-Projekt 6454, 1997–1998), overall funding approx. 0.55 Mio.ATS. Joint project with Department of General Electrotechnical Engineering and Electronics (TU-Wien).
- Project proposal and management project *Distributed Embedded Systems under OSE* (2000–2001) [195]. Internal project of TU-Wien, overall funding approx. 1.5 Mio.ATS.
- Participation in proposal setup, consortium agreement negotiation and internal setup + supervision EU FP-6 Integrated Project *Automated proof-based System and Software Engineering for Real-Time systems* (ASSERT, IST-004033, 2004–2006) [24]. Collaboration with INRIA Rocquencourt, EADS, Dassault Aviation, Alcatel Space etc.; Coordinator European Space Agency. Total costs 15 Mio.EUR, funding TU approx. EUR 220.000,–.
- Project proposal and supervision BM:VIT FIT-IT-Project *Seamless Campus: Distance Labs* (SC-DL, Proj.No. 808210, 2004-2006). Embedded Systems accompanying measures project, funding EUR 350.000,–.
- Supervision BM:VIT FIT-IT-Project *Distributed Computing in the Presence of Bounded Asynchrony* (DCBA, Proj.No. 808198, 2004). Embedded Systems PhD project (Josef Widder), funding EUR 63.000,–.
- Project proposal and management FWF-project *Asynchronous Distributed Algorithms in the* Θ*-Model* (THETA, P17757, 2005–2009) [179, 159], overall funding approx. EUR 190.000,–.
- Project definition and proposal setup (jointly with A. Steininger und G. Fuchs) BM:VIT FIT-IT project *Distributed Algorithms for Robust Tick Synchronization* (DARTS, proj.no. 809456, 2005-2008, project head A. Steininger) [172]. Joint project with Austrian Aerospace, total costs EUR 700.000,–. Best project award at the 4th FIT-IT Embedded Systems call.
- Project definition and proposal setup FWF-project *Fault-Tolerant Distributed Algorithms in Sparse Ad Hoc Wireless Networks* (SPAWN, Proj.Nr. P18264, 2005–2009, project head Bettina Weiss) [173], overall funding approx. EUR 185.000,–.
- Supervision BM:VIT FIT-IT project *Transient Fault-Tolerance* (TRAFT, Proj.No. 812205, 2006–2010). Embedded Systems PhD project (Martin Biely), funding EUR 72.000,–.
- Supervision BM:VIT FIT-IT project *Fault-Injection in Distributed Systems* (FIDIS, Proj.Nr. 813441, 2007–2010). Embedded Systems PhD project (Christian Trödhandl), funding EUR 72.000,–.
- Supervision BM:VIT FIT-IT project *Fault-Models for Engineering* (FAME, Proj.Nr. 816454, 2008-2011., project head Bettina Weiss). Embedded Systems PhD pojekt (Günther Gridling), funding EUR 72.000,–.
- Project proposal and management FWF projekt *Partially Synchronous Distributed Real-Time Systems*(PSRTS, proj.no. P20529, 2008–2013) [160], total funding EUR 310.000,–.
- Project definition and proposal setup (with A. Steininger and H. Zimmermann) FWF-Projekt *Fault-Tolerant Asynchronous Logic* (FATAL, proj.no. P21694, 2009–now) [158], total funding EUR 451.000,–. Joint project with Institute of Electrical Measurements and Circuit Design and TU Wien's Atominstitut.
- Collaborative project definition and proposal writing (jointly with R. Bloem/TU-Graz, T. Henzinger, K. Chatterjee/IST Austria, A. Biere/Uni Linz, Ch. Kirsch/Uni Salzburg, L. Kovacs, H. Veith, U. Egly/TU Wien) National Research Network *Rigorous Systems Engineering* (RiSE, Austrian Science Fund FWF Proj.Nr. S11405-N23, 2011-now), Sub-Projekt *Reconciling Distributed Computing and Real-Time Systems*, PP05 funding EUR 284.000,–.

  Project definition and proposal writing 2nd phase of RiSE NFN, (SHiNE, FWF proj.no. S11405-N23, 2015–now). Continuation of sub-project PP05, jointly with E. Bartocci (sub-task leader); PP05 funding EUR 465.220,–.
- Project definition and proposal setup (jointly with M. Függer) FWF project *Self-stabilizing Byzantine Fault-Tolerant Distributed Algorithms for Integrated Circuits* (SIC, proj.no. P26436, project head M. Függer, 2013–now) [151], total funding EUR 349.000,–.
- Project definition and proposal setup (jointly with A. Steininger und H. Zimmermann) FWF project *Accelerator-based Experimental Analysis and Simulation Modeling of Single-Event Transients in VLSI Circuits* (EASET, proj.no. P26435, project head A. Steininger, 2014–lfd.) [152], total funding EUR 443.000,–. Joint project with Institute of Electrical Measurements and Circuit Design at TU Wien.
- Project definition and proposal writing FWF project *Gracefully Degrading Agreement in Directed Dynamic Networks* (ADynNet, proj.no. P28182, 2016–now) [145], total funding EUR 349.755,–.
- Collaborative proposal writing for the 2nd phase of the FWF Doctoral Program *Logics in Computer Science* (LogiCS, FWF Proj.Nr. W1255, 2018–now). Full member LogiCS factulty, funding (2 PhD positions) approx. EUR 350.000,–.

Detailed References

References

[1] Martin Biely, Peter Robinson, Ulrich Schmid, Manfred Schwarz, and Kyrill Winkler. Gracefully degrading consensus and k-set agreement in directed dynamic networks. *Theoretical Computer Science*, 2018. (in press).

[2] Krishnendu Chatterjee, Andreas Pavlogiannis, Alexander Kößler, and Ulrich Schmid. Automated competitive analysis of real-time scheduling with graph games. *Real-Time Systems*, 54(1):166–207, Jan 2018.

[3] Varadan Savulimedu Veeravalli, Andreas Steininger, and Ulrich Schmid. A versatile architecture for long-term monitoring of single-event transient durations. *Microprocessors and Microsystems*, 53(Supplement C):130 – 144, 2017.

[4] Matthias Függer, Thomas Nowak, and Ulrich Schmid. Unfaithful glitch propagation in existing binary circuit models. *IEEE Transactions on Computers*, 65(3):964–978, March 2016.

[5] Danny Dolev, Matthias Függer, Christoph Lenzen, Martin Perner, and Ulrich Schmid. HEX: Scaling honeycombs is easier than scaling clock trees. *Journal of Computer and System Sciences*, 82(5):929–956, aug 2016.

[6] Matthias Függer, Alexander Kößler, Thomas Nowak, Ulrich Schmid, and Martin Zeiner. The effect of forgetting on the performance of a synchronizer. *Performance Evaluation*, 93:1–16, 2015.

[7] Andreas Steininger, Horst Zimmermann, Axel Jantsch, Michael Hofbauer, Ulrich Schmid, Kurt Schweiger, and Varadan Savulimedu Veeravalli. Building reliable systems-on-chip in nanoscale technologies. *Elektrotechnik und Informationstechnik*, 132(6):301–306, 2015.

[8] Danny Dolev, Matthias Függer, Ulrich Schmid, and Christoph Lenzen. Fault-tolerant algorithms for tick-generation in asynchronous logic: Robust pulse generation. *Journal of the ACM*, 61(5), April 2014.

[9] Danny Dolev, Matthias Függer, Christoph Lenzen, Markus Posch, Ulrich Schmid, and Andreas Steininger. Rigorously modeling self-stabilizing fault-tolerant circuits: An ultra-robust clocking scheme for systems-on-chip. *Journal of Computer and System Sciences*, 80(4):860–900, 2014.

[10] Heinrich Moser and Ulrich Schmid. Reconciling fault-tolerant distributed algorithms and real-time computing. *Distributed Computing*, 27:203–230, 2014.

[11] Martin Biely, Peter Robinson, and Ulrich Schmid. The generalized loneliness detector and weak system models for k-set agreement. *IEEE Transactions on Parallel and Distributed Systems*, 25(4):1078–1088, April 2014.

[12] Michael Hofbauer, Kurt Schweiger, Horst Zimmermann, Ulrich Giesen, Frank Langner, Ulrich Schmid, and Andreas Steininger. Supply voltage dependent on-chip single event transient pulse shape measurements in 90 nm bulk CMOS under alpha irradiation. *IEEE Transactions on Nuclear Science*, 60(4):2640–2646, August 2013.

[13] Varadan Savulimedu Veeravalli, Thomas Polzer, Andreas Steininger, Ulrich Schmid, Michael Hofbauer, Kurt Schweiger, Horst Dietrich, Kerstin Schneider-Hornstein, Horst Zimmermann, Kay-Obbe Voss, Bruno Merk, and Michael Hajek. An infrastructure for accurate characterization of single-event transients in digital circuits. *Microprocessors and Microsystems*, 37(8-A):772–791, 2013.

[14] Matthias Függer and Ulrich Schmid. Reconciling fault-tolerant distributed computing and systems-on-chip. *Distributed Computing*, 24(6):323–355, 2012.

[15] Michael Hofbauer, Kurt Schweiger, Horst Dietrich, Horst Zimmermann, Kay-Obbe Voss, Bruno Merk, Ulrich Schmid, and Andreas Steininger. Pulse shape measurements by on-chip sense amplifiers of single event transients propagating through a 90 nm bulk CMOS inverter chain. *IEEE Transactions on Nuclear Science*, 59(6):2778–2784, December 2012.

[16] Martin Biely, Ulrich Schmid, and Bettina Weiss. Synchronous consensus under hybrid process and link failures. *Theoretical Computer Science*, 412(40):5602 – 5630, 2011. http://dx.doi.org/10.1016/j.tcs.2010.09.032.

[17] Peter Robinson and Ulrich Schmid. The Asynchronous Bounded-Cycle Model. *Theoretical Computer Science*, 412(40):5580–5601, 2011. http://dx.doi.org/10.1016/j.tcs.2010.08.001.

[18] Bernd Thallner, Heinrich Moser, and Ulrich Schmid. Topology control for fault-tolerant communication in wireless ad-hoc networks. *Wireless Networks*, 16(2):387–404, 2010.

[19] Ulrich Schmid, Bettina Weiss, and Idit Keidar. Impossibility results and lower bounds for consensus under link failures. *SIAM Journal on Computing*, 38(5):1912–1951, 2009.

[20] Josef Widder and Ulrich Schmid. The Theta-Model: Achieving synchrony without clocks. *Distributed Computing*, 22(1):29–47, April 2009.

[21] Martin Hutle, Dahlia Malkhi, Ulrich Schmid, and Lidong Zhou. Chasing the weakest system model for implementing omega and consensus. *IEEE Transactions on Dependable and Secure Computing*, 6(4):269–281, 2009.

[22] Josef Widder and Ulrich Schmid. Booting clock synchronization in partially synchronous systems with hybrid process and link failures. *Distributed Computing*, 20(2):115–140, August 2007.

[23] Ulrich Schmid, Andreas Steininger, and Manfred Sust. FIT-IT-Projekt DARTS: Dezentrale fehlertolerante Taktgenerierung. *Elektrotechnik & Informationstechnik (e&i) 1-2/07, 2007*, Jan. 2007. (Invited paper).

[24] Hermann Kopetz, Roman Obermaisser, and Ulrich Schmid. Dependable embedded systems research at TU Vienna. *e & i*, 1/2:33–37, January/February 2005. (Invited paper).

[25] Ulrich Schmid. Applied research: A scientist's perspective. *Annual Reviews in Control*, 25:183–190, 2001. (Reprinted from [109]).

[26] U. Schmid, J. Klasek, T. Mandl, H. Nachtnebel, G. R. Cadek, and N. Kerö. A Network Time Interface M-Module for distributing GPS-time over LANs. *J. Real-Time Systems*, 18(1):24–57, January 2000.

[27] Ulrich Schmid and Klaus Schossmaier. How to reconcile fault-tolerant interval intersection with the Lipschitz condition. *Distributed Computing*, 14(2):101 – 111, May 2001.

[28] Ulrich Schmid. Orthogonal accuracy clock synchronization. *Chicago Journal of Theoretical Computer Science*, 2000(3):3–77, 2000.

[29] Ulrich Schmid and Klaus Schossmaier. Interval-based clock synchronization with optimal precision. *Information and Computation*, 186(1):36–77, October 2003.

[30] Ulrich Schmid. Hochgenaue Uhrensynchronisation über LANs. *Elektronikschau*, 10:20–23, October 1997.

[31] Klaus Schossmaier, Ulrich Schmid, Martin Horauer, and Dietmar Loy. Specification and implementation of the Universal Time Coordinated Synchronization Unit (UTCSU). *Real-Time Systems*, 12(3):295–327, May 1997.

[32] Ulrich Schmid and Klaus Schossmaier. Interval-based clock synchronization. *Real-Time Systems*, 12(2):173–228, March 1997.

[33] Ulrich Schmid. Synchronized Universal Time Coordinated for distributed real-time systems. *Control Engineering Practice*, 3(6):877–884, 1995. (Reprint from [128]).

[34] Ulrich Schmid and Alfred Pusterhofer. SSCMP: The sequenced synchronized clock message protocol. *Computer Networks and ISDN Systems*, 27:1615–1632, 1995.

[35] Ulrich Schmid. Static priority scheduling of aperiodic real-time tasks. *Random Structures and Algorithms*, 10(1-2):257–303, 1997.

[36] Ulrich Schmid. Random trees in queueing systems with deadlines. *Theoretical Computer Science*, 144(1-2):277–314, 1995. (Habilitationsschrift).

[37] Harald Haberstroh, Wolfgang Kastner, and Ulrich Schmid. M-Module im Didaktik-Einsatz. *Elektronik Industrie*, 10:90–92, 1994.

[38] Jürgen Meyer and Ulrich Schmid. Zeit im Bild. *Elektronikschau*, 3:28–30, March 1995.

[39] Ulrich Schmid. Monitoring distributed real-time systems. *Real-Time Systems*, 7:33–56, 1994.

[40] Michael Drmota and Ulrich Schmid. Exponential limiting distributions in queueing systems with deadlines. *SIAM Journal on Applied Mathematics*, 53(1):301–318, 1993.

[41] Michael Drmota and Ulrich Schmid. The analysis of the expected successful operation time of slotted ALOHA. *IEEE Transactions on Information Theory*, 39(5):1567–1577, 1993.

[42] Ulrich Schmid and Johann Blieberger. On nonpreemptive LCFS scheduling with deadlines. *Journal of Algorithms*, 18:124–158, 1995.

[43] Johann Blieberger and Ulrich Schmid. FCFS scheduling in a hard real-time environment under rush-hour conditions. *BIT*, 32(3):370–383, 1992.

[44] Ulrich Schmid. The average CRI-length of a controlled ALOHA collision resolution algorithm. *Theoretical Computer Science*, 108:291–310, 1993.

[45] Johann Blieberger and Ulrich Schmid. Preemptive LCFS scheduling in hard real time applications. *Performance Evaluation*, 15(3):203–215, 1992.

[46] Ulrich Schmid and Johann Blieberger. Some investigations on FCFS scheduling in hard real time applications. *Journal of Computers and System Sciences*, 45:493–512, 1992.

[47] Ulrich Schmid. On the asymptotics of the average CRI-length of the slotted ALOHA collision resolution algorithm. *Applied Mathematics and Computation*, 48:59–70, 1992.

[48] Ulrich Schmid. On a tree collision resolution algorithm in presence of capture. *RAIRO Informatique Theorique et Applications/Theoretical Informatics and Applications*, 26(2):163–197, 1992.

[49] Franz Beranek and Ulrich Schmid. Assembler mit Pascalelementen. *Elektronikschau*, 2:32–34, February 1983.

[50] C. Fan, Y. Meng, J. Maier, E. Bartocci, S. Mitra, and U. Schmid. Verifying nonlinear analog and mixed-signal circuits with inputs. In *Proceedings of the IFAC Conference on Analysis and Design of Hybrid Systems (ADHS'18)*, 2018. (to appear).

[51] Matthias Függer, Jürgen Maier, Robert Najvirt, Thomas Nowak, and Ulrich Schmid. A faithful binary circuit model with adversarial noise. In *Proceeding of the 2018 Design, Automation & Test in Europe (DATE)*, DATE'18, pages 1333–1338, 2018.

[52] Manfred Schwarz, Kyrill Winkler, and Ulrich Schmid. Fast consensus under eventually stabilizing message adversaries. In *Proceedings of the 17th International Conference on Distributed Computing and Networking*, ICDCN '16, pages 7:1–7:10, New York, NY, USA, 2016. ACM.

[53] Daniel Pfleger and Ulrich Schmid. A framework for connectivity monitoring in wireless sensor networks. In *Proceedings 10th International Conference on Sensor Technlogies and Applications (SENSORCOMM'16)*, pages 40–48. IARIA, 2016. https://www.thinkmind.org/download.php?articleid=sensorcomm_2016_3_10_10013.

[54] Matthias Függer, Robert Najvirt, Thomas Nowak, and Ulrich Schmid. Towards binary circuit models that faithfully capture physical solvability. In *Proceedings of the 2015 Design, Automation & Test in Europe Conference & Exhibition*, DATE '15, pages 1455–1460, San Jose, CA, USA, 2015. EDA Consortium.

[55] Robert Najvirt, Ulrich Schmid, Michael Hofbauer, Matthias Függer, Thomas Nowak, and Kurt Schweiger. Experimental validation of a faithful binary circuit model. In *Proceedings of the 25th Edition on Great Lakes Symposium on VLSI*, GLSVLSI '15, pages 355–360, New York, NY, USA, 2015. ACM.

[56] Martin Biely, Peter Robinson, Ulrich Schmid, Manfred Schwarz, and Kyrill Winkler. Gracefully degrading consensus and k-set agreement in directed dynamic networks. In *Revised selected papers Third International Conference on Networked Systems (NETYS'15)*, Springer LNCS 9466, pages 109–124, Agadir, Morocco, 2015. Springer International Publishing.

[57] Varadan Savulimedu Veeravalli, Andreas Steininger, and Ulrich Schmid. Measuring SET pulsewidths in logic gates using digital infrastructure. In *Proceedings Internationsal Symposium on Quality of Electronic Design (ISQED'14)*, pages 236–242, 2014.

[58] Manfred Schwarz, Kyrill Winkler, Ulrich Schmid, Martin Biely, and Peter Robinson. Brief announcement: Gracefully degrading consensus and k-set agreement under dynamic link failures. In *Proceedings of the 33th ACM SIGACT-SIGOPS Symposium on Principles of Distributed Computing*, PODC '14, pages 341–343, New York, NY, USA, 2014. ACM.

[59] Krishnendu Chatterjee, Andreas Pavlogiannis, Alexander Kößler, and Ulrich Schmid. A framework for automated competitive analysis of on-line scheduling of firm-deadline tasks. In *Proceedings of the IEEE 35th IEEE Real-Time Systems Symposium, RTSS 2014, Rome, Italy, December 2-5, 2014*, pages 118–127, 2014.

[60] Matthias Függer, Thomas Nowak, and Ulrich Schmid. Unfaithful glitch propagation in existing binary circuit models. In *Proceedings 19th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC'13)*, pages 191–199. IEEE Computer Society, 2013.

[61] Krishnendu Chatterjee, Alexander Kößler, and Ulrich Schmid. Automated analysis of real-time scheduling using graph games. In *Proceedings of the 16th ACM international conference on Hybrid Systems: Computation and Control*, HSCC '13, pages 163–172, New York, NY, USA, 2013. ACM.

[62] Annu John, Igor Konnov, Ulrich Schmid, Helmut Veith, and Josef Widder. Towards modeling and model checking fault-tolerant distributed algorithms. In *Proceedings 20th International Symposium on Model Checking Software (SPIN'13), Springer LNCS 7976*, pages 209–226. Springer, 2013.

[63] Annu John, Igor Konnov, Ulrich Schmid, Helmut Veith, and Josef Widder. Brief announcement: Parameterized model checking of fault-tolerant distributed algorithms by abstraction. In *Proceedings ACM Symposium on Principles of Distributed Computing (PODC'13)*, pages 119–121. ACM, 2013.

[64] Danny Dolev, Matthias Függer, Christoph Lenzen, Martin Perner, and Ulrich Schmid. HEX: Scaling Honeycombs is Easier than Scaling Clock Trees. In *Proc. 25th ACM Symp. on Parallelism in Algorithms and Architect ures (SPAA'13)*, pages 164–175, 2013.

[65] Martin Perner, Martin Sigl, Ulrich Schmid, and Christoph Lenzen. Byzantine self-stabilizing clock distribution with HEX: Implementation, simulation, clock multiplication. In *Proc. Sixth IARIA International Conference on Dependability (DEPEND'13)*, pages 6–15, 2013.

[66] Matthias Függer, Markus Hofstätter, Christoph Lenzen, and Ulrich Schmid. Efficient construction of global time in SoCs despite arbitrary faults. In *Proc. 16th Euromicro Conference on Digital System Design (DSD'13)*, pages 142–151, 2013.

[67] Annu John, Igor Konnov, Ulrich Schmid, Helmut Veith, and Josef Widder. Parameterized model checking of fault-tolerant distributed algorithms by abstraction. In *Proceedings Formal Methods in Computer-Aided Design (FMCAD'13)*, pages 201–209. IEEE, 2013.

[68] Matthias Függer, Alexander Kößler, Thomas Nowak, Ulrich Schmid, and Martin Zeiner. The effect of forgetting on the performance of a synchronizer. In *Proceedings ALGOSENSORS'13, Springer LNCS 8243*, pages 185–200. Springer, 2013.

[69] Martin Biely, Peter Robinson, and Ulrich Schmid. Agreement in directed dynamic networks. In *Proceedings 19th International Colloquium on Structural Information and Communication Complexity (SIROCCO'12)*, LNCS 7355, pages 73–84. Springer-Verlag, 2012.

[70] Varadan Savulimedu Veeravalli, Thomas Polzer, Andreas Steininger, and Ulrich Schmid. Architecture and design analysis of a digital single-event transient/upset measurement chip. In *Proceedings 15th Euromicro Symposium on Digital System Design: Architectures, Methods and Tools (DSD'12)*, pages 8–17, sep 2012. (best paper award).

[71] Danny Dolev, Matthias Függer, Christoph Lenzen, and Ulrich Schmid. Fault-tolerant algorithms for tick-generation in asynchronous logic: Robust pulse generation - [extended abstract]. In *Proceedings 13th International Symposium on Stabilization, Safety, and Security of Distributed Systems (SSS'11), Springer LNCS 6976*, pages 163–177, 2011.

[72] Martin Biely, Peter Robinson, and Ulrich Schmid. Easy impossibility proofs for k-set agreement in message passing systems. In *Proceedings of the 30th Annual ACM Symposium on Principles of Distributed Computing (PODC'11)*, pages 227–228. ACM, 2011.

[73] Martin Biely, Peter Robinson, and Ulrich Schmid. Easy impossibility proofs for k-set agreement in message passing systems. In *Proceedings 15th International Conference on Principles of Distributed Systems (OPODIS'11), Springer LNCS 7109*, pages 299–312, 2011.

[74] Martin Biely, Peter Robinson, and Ulrich Schmid. Solving k-set agreement with stable skeleton graphs. In *IPDPS Workshops*, pages 1488–1495, 2011. (also available in arxiv:1102.4423).

[75] Heinrich Moser and Ulrich Schmid. Reconciling fault-tolerant distributed algorithms and real-time computing. In *18th International Colloquium on Structural Information and Communication Complexity (SIROCCO)*, LNCS 6796, pages 42–53, Berlin, Heidelberg, 2011. Springer-Verlag.

[76] Matthias Függer, Andreas Dielacher, and Ulrich Schmid. How to speed-up fault-tolerant clock generation in vlsi systems-on-chip via pipelining. In *Proceedings Eighth European Dependable Computing Conference (EDCC'10)*, pages 230–239, 2010.

[77] Alois Goiser, Samar Khattab, Gerhard Fassl, and Ulrich Schmid. A new robust interference reduction scheme for low complexity direct-sequence spread-spectrum receivers: Optimization. In *Proceedings 3rd International IEEE Conference on Communication Theory, Reliability, and Quality of Service (CTRQ'10)*, pages 32–36, Athens, Greece, June 2010.

[78] Alois Goiser, Samar Khattab, Gerhard Fassl, and Ulrich Schmid. A new robust interference reduction scheme for low complexity direct-sequence spread-spectrum receivers: Performance. In *Proceedings 3rd International IEEE Conference on Communication Theory, Reliability, and Quality of Service (CTRQ'10)*, pages 15–21, Athens, Greece, June 2010.

[79] Ulrich Schmid. Synchrony and time in fault-tolerant distributed algorithms - (invited tutorial). In *Proceedings Formal Modeling and Analysis of Timed Systems Conference (FORMATS 2010)*, volume 6246 of *Lecture Notes in Computer Science*, page 46. Springer, 2010.

[80] Alexander K"ossler, Heinrich Moser, and Ulrich Schmid. Real-time analysis of round-based distributed algorithms. In *Proceedings of the 1st International Real-Time Scheduling Open Problems Seminar (RTSOPS'10), in conjunction with 22nd Euromicro Conference on Real-Time Systems (ECRTS'10)*, pages 9–11, Jul. 2010. Published as as TR under https://www.cs.york.ac.uk/ftpdir/reports/2010/YCS/455/YCS-2010-455.pdf.

[81] Andreas Dielacher, Matthias Fuegger, and Ulrich Schmid. Brief announcement: How to speed-up fault-tolerant clock generation in VLSI systems-on-chip via pipelining. In *Proceedings of the 28th ACM Symposium on Principles of Distributed Computing (PODC'09)*, page 423. ACM Press, August 2009. An extended version is available as RR 15/2009, Institut für Technische Informatik, TU-Wien, http://www.vmars.tuwien.ac.at/documents/extern/2571/techreport.pdf.

[82] Matthias Fuegger, Gottfried Fuchs, Ulrich Schmid, and Andreas Steininger. On the stability and robustness of non-synchronous circuits with timing loops. *3rd Workshop on Dependable and Secure Nanocomputing*, Jun. 2009.

[83] Martin Biely, Peter Robinson, and Ulrich Schmid. Weak synchrony models and failure detectors for message passing k-set agreement. In *Proceedings of the 23rd International Symposium on Distributed Computing (DISC'09)*, pages 260–261, 2009.

[84] Martin Biely, Peter Robinson, and Ulrich Schmid. Weak synchrony models and failure detectors for message passing k-set agreement. In *Proceedings of the International Conference on Principles of Distributed Systems (OPODIS'09)*, LNCS, pages 285–299, Nimes, France, Dec 2009. Springer Verlag.

[85] Ulrich Schmid. Keynote: Distributed algorithms and VLSI. In *Proceedings of the 10th International Symposium on Stabilization, Safety, and Security of Distributed Systems (SSS'08)*, volume 5340 of *Lecture Notes in Computer Science*, page 3, Detroit, USA, November 2008. Springer Verlag. (http://www.vmars.tuwien.ac.at/documents/extern/2467/sss08.pdf).

[86] Peter Robinson and Ulrich Schmid. Brief announcement: The asynchronous bounded-cycle model. In *Proceedings of the 27th ACM Symposium on Principles of Distributed Computing (PODC'08)*, page 423. ACM Press, August 2008. (extended version appeared at SSS'08).

[87] Peter Robinson and Ulrich Schmid. The Asynchronous Bounded-Cycle Model. In *Proceedings of the 10th International Symposium on Stabilization, Safety, and Security of Distributed Systems (SSS'08)*, volume 5340 of *Lecture Notes in Computer Science*, pages 246–262, Detroit, USA, November 2008. Springer Verlag. (Best Paper Award).

[88] Gottfried Fuchs, Matthias Fuegger, Ulrich Schmid, and Andreas Steininger. Mapping a fault-tolerant distributed algorithm to systems on chip. In *11th Euromicro conference on Digital System Design Architectures, Methods and Tools (DSD'08)*, pages 242–249, Parma, Italy, September 2008.

[89] Heinrich Moser and Ulrich Schmid. Optimal deterministic remote clock estimation in real-time systems. In *Proceedings of the International Conference on Principles of Distributed Systems (OPODIS)*, pages 363–387, Luxor, Egypt, December 2008.

[90] Ulrich Schmid, Andreas Steininger, and Helmut Veith. Towards a systematic design of fault-tolerant asynchronous circuits. In *Proceedings GMM/GI/ITG-Fachtagung Zuverlässigkeit und Entwurf*, pages 173–174, Munich, Germany, March 2007. VDE-Verlag, Berlin, Offenbach.

[91] Ulrich Schmid. Keynote: A perspective of fault-tolerant clock synchronization. In *Proceedings of the IEEE International Symposium on Precision Clock Synchronization for Measurement, Control and Communication (ISPCS'07)*, page vii, Vienna, Austria, October 2007. (http://www.vmars.tuwien.ac.at/documents/extern/2339/ispcs.pdf).

[92] Gottfried Fuchs, Julian Grahsl, Ulrich Schmid, Andreas Steininger, and Gerald Kempf. Threshold Modules – Die Schlüsselelemente zur Verteilten Generierung eines Fehlertoleranten Taktes. In *Proceedings of the Austrian National Conference on the Design of Integrated Circuits and Systems (Austrochip 2006)*, pages 149–156, Vienna, October 2006.

[93] Matthias Fuegger, Ulrich Schmid, Gottfried Fuchs, and Gerald Kempf. Fault-Tolerant Distributed Clock Generation in VLSI Systems-on-Chip. In *Proceedings of the Sixth European Dependable Computing Conference (EDCC-6)*, pages 87–96. IEEE Computer Society Press, October 2006.

[94] Martin Hutle, Dahlia Malkhi, Ulrich Schmid, and Lidong Zhou. Brief announcement: Chasing the weakest system model for implementing omega and consensus. In *Proceedings Eighth International Symposium on Stabilization, Safety, and Security of Distributed Systems (SSS 2006)*, LNCS, pages 576–577, Dallas, USA, Nov. 2006. Springer Verlag.

[95] Heinrich Moser and Ulrich Schmid. Optimal clock synchronization revisited: Upper and lower bounds in real-time systems. In *Proceedings of the International Conference on Principles of Distributed Systems (OPODIS)*, LNCS 4305, pages 95–109, Bordeaux & Saint-Emilion, France, Dec 2006. Springer Verlag.

[96] Heinrich Moser and Ulrich Schmid. Reconciling distributed computing models and real-time systems. In *Proceedings Work in Progress Session of the 27th IEEE Real-Time Systems Symposium (RTSS'06)*, pages 73–76, Rio de Janeiro, Brazil, Dec 2006.

[97] Andreas Steininger, Matthias Fuegger, Ulrich Schmid, and Gottfried Fuchs. Fault-Tolerant Algorithms on SoCs - A case study. In *Supplemental Proceedings of the International Conference on Dependable Systems and Networks (DSN'06)*, pages 190–191, Philadelphia, USA, June 2006.

[98] Christof Fetzer, Ulrich Schmid, and Martin Süßkraut. On the possibility of consensus in asynchronous systems with finite average response times. In *Proceedings of the 25th International Conference on Distributed Computing Systems (ICDCS'05)*, pages 271–280, Washington, DC, USA, June 2005. IEEE Computer Society.

[99] Josef Widder, Gérard Le Lann, and Ulrich Schmid. Failure detection with booting in partially synchronous systems. In *Proceedings of the 5th European Dependable Computing Conference (EDCC-5)*, volume 3463 of *LNCS*, pages 20–37, Budapest, Hungary, April 2005. Springer Verlag.

[100] Martin Biely, Gérard Le Lann, and Ulrich Schmid. Proof-based systems engineering using a virtual system model. In *Proceedings 2nd International Service Availability Symposium (ISAS'05)*, number 3694 in Lecture Notes in Computer Science, pages 164–179, Berlin, Germany, April 2005. Springer.

[101] Josef Widder and Ulrich Schmid. Achieving synchrony without clocks. Research Report 49/2005, Technische Universität Wien, Institut für Technische Informatik, 2005. (to appear in Distributed Computing, 2009).

[102] Christof Fetzer and Ulrich Schmid. Brief announcement: On the possibility of consensus in asynchronous systems with finite average response times. In *Proceedings of the 23th ACM Symposium on Principles of Distributed Computing (PODC'04)*, page 402, Boston, Massachusetts, 2004.

[103] Ulrich Schmid and Christof Fetzer. Randomized asynchronous consensus with imperfect communications. In *22nd Symposium on Reliable Distributed Systems (SRDS'03)*, pages 361–370, Florence, Italy, October 6–8, 2003.

[104] Roland Höller, Martin Horauer, Günther Gridling, Nikolaus Kerö, Ulrich Schmid, and Klaus Schossmaier. SynUTC - high precision time synchronization over Ethernet networks. In *Proceedings of the 8th Workshop on Electronics for LHC Experiments (LECC'02)*, pages 428–432, Colmar, France, September 9–13, 2002.

[105] Martin Horauer, Ulrich Schmid, Klaus Schossmaier, Roland Höller, and Nikolaus Kerö. PSynUTC — evaluation of a high precision time synchronization prototype system for Ethernet LANs. In *Proceedings of the 34th IEEE Precise Time and Time Interval Systems and Application Meeting (PTTI'02)*, pages 263–278, Reston, Virginia, December 2002.

[106] Bettina Weiss and Ulrich Schmid. Consensus with written messages under link faults. In *20th Symposium on Reliable Distributed Systems (SRDS'01)*, pages 194–197, New Orleans, LA, USA, October 28–31, 2001.

[107] Ulrich Schmid, Bettina Weiss, and John Rushby. Formally verified Byzantine agreement in presence of link faults. In *22nd International Conference on Distributed Computing Systems (ICDCS'02)*, pages 608–616, Vienna, Austria, July 2-5, 2002.

[108] Ulrich Schmid. High-accuracy time services and fault-tolerant clock synchronization. In *37th IFIP WG10.4 Annual Meeting (Workshop on "Time and Dependability"*, pages 39–57, Martinique, France, January 21–25, 2000. (Invited presentation).

[109] Ulrich Schmid. Applied research: A scientist's perspective. In *Proceedings joint 25th IFAC/IFIP Workshop on Real-Time Programming (WRTP'00) and Workshop on Algorithms and Architectures for Real-Time Control (AARTC'00)*, pages 5–12, Palma de Mallorca, Spain, May 2000. (Invited plenary speech).

[110] Martin Horauer, Nikolaus Kerö, and Ulrich Schmid. A network interface for highly accurate clock synchronization. In W. Maierwieser and K.G. Posch, editors, *Proceedings AUSTROCHIP'00*, pages 93–101, Graz, Austria, October 2000. ISBN 3-9501349-0-5.

[111] Ulrich Schmid. How to model link failures: A perception-based fault model. In *Proceedings of the International Conference on Dependable Systems and Networks (DSN'01)*, pages 57–66, Göteborg, Sweden, July 1–4, 2001.

[112] Wolfgang Kastner and Ulrich Schmid. How to teach matters of modern control systems to computer science students? In *Proceedings 5th IFAC Symposium on Advances in Control Education (ACE'00)*, Sea World Nara Resort, Australia, December 2000.

[113] Ulrich Schmid, Bettina Weiss, Günther Gridling, and Klaus Schossmaier. A unified approach for simulation and experimental evaluation of fault-tolerant distributed systems. In *Proceedings of the IASTED International Conference on Applied Modelling and Simulation (AMS'99)*, pages 43–48, Cairns, Queensland, Australia, September 1–3, 1999.

[114] Ulrich Schmid, Martin Horauer, and Nikolaus Kerö. How to distribute GPS-time over COTS-based LANs. In *Proceedings of the 31th IEEE Precise Time and Time Interval Systems and Application Meeting (PTTI'99)*, pages 545–560, Dana Point, California, December 1999.

[115] Bettina Weiss, Günther Gridling, Ulrich Schmid, and Klaus Schossmaier. The SimUTC fault-tolerant distributed systems simulation toolkit. In *Proceedings 7th International Symposium on Modeling, Analysis and Simulation of Computer and Telecommunication Systems (MASCOTS'99)*, pages 68–75, College Park, MD, USA, October 24–28, 1999.

[116] Ulrich Schmid and Herbert Nachtnebel. Experimental evaluation of high-accuracy time distribution in a COTS-based Ethernet LAN. In *Proceedings 24th IFAC/IFIP Workshop on Real-Time Programming (WRTP'99)*, pages 59–68, Schloß Dagstuhl, Germany, May/June 1999.

[117] Ulrich Schmid. Internet-based real-time computing. In *Proceedings 22nd Annual International Computer Software & Applications Conference (COMPSAC'98)*, pages 338–342, Vienna, Austria, August 1998.

[118] Herbert Nachtnebel, Nikolaus Kerö, Gerhard R. Cadek, Thomas Mandl, and Ulrich Schmid. Rapid Prototyping mit programmierbarer Logik: Ein Fallbeispiel. In *Proceedings AUSTROCHIP'98*, pages 99–104, Wiener Neustadt, Austria, October 1998.

[119] Dieter Höchtl and Ulrich Schmid. Long-term evaluation of GPS timing receiver failures. In *Proceedings of the 29th IEEE Precise Time and Time Interval Systems and Application Meeting (PTTI'97)*, pages 165–180, Long Beach, California, December 1997.

[120] Ulrich Schmid and Wolfgang Kastner. *DOBOS: Ein Distributed Object-Based Operating System für Soft Real-Time Systems*, pages 3–13. Viehweg-Verlag, 1996. (Reprint of [123]).

[121] Wolfgang Kastner and Ulrich Schmid. Process control engineering for computer science students. In *Proceedings 4th IFAC Symposium on Advances in Control Education (ACE'97)*, pages 289–295, Istambul, Turkey, July 1997.

[122] Martin Horauer, Ulrich Schmid, and Klaus Schossmaier. NTI: A Network Time Interface M-Module for high-accuracy clock synchronization. In *Proceedings 6th International Workshop on Parallel and Distributed Real-Time Systems (WPDRTS'98)*, pages 1067–1076, Orlando, Florida, March 30 – April 3 1998.

[123] Ulrich Schmid and Wolfgang Kastner. DOBOS: Ein Distributed Object-Based Operating System für Soft Real-Time Systems. In *Proceedings Echtzeit'94*, pages 130–136, Hamburg, Germany, 1994.

[124] Wolfgang A. Halang, F.-J. Koller, Ulrich Schmid, and M. Witte. Untersuchung des Zeitverhaltens Verteilter Echtzeitsysteme. In *Proceedings Echtzeit'95*, pages 101–107, June 1995.

[125] Ulrich Schmid, Wolfgang Kastner, and Harald Haberstroh. Process control education for computer science: From fiction back to facts. In *Proceedings TEMPUS JEP 07759 - MODIFY Workshop on Automation and Control Engineering in Higher Education*, pages 135–147, Vienna, Austria, July 1995.

[126] Ulrich Schmid, Harald Haberstroh, and Stefan Stöckler. Process control education for computer science: Facts and fiction. In *Proceedings SEFI/TEMPUS JEP 2011 - IMPACT Workshop on Computer Science Topics for Control Engineering Education*, pages 13–22, Vienna, Austria, September 1993.

[127] Ulrich Schmid. *Monitoring in verteilten Echtzeitsystemen*, pages 265–276. Viehweg-Verlag, 1994. (Reprint of [133]).

[128] Ulrich Schmid. Synchronized UTC for distributed real-time systems. In *Proceedings 19th IFAC/IFIP Workshop on Real-Time Programming (WRTP'94)*, pages 101–107, Lake Reichenau, Germany, 1994.

[129] Ulrich Schmid and Stefan Stöckler. A versatile monitoring system for distributed real-time systems. In *Proceedings 11th IFAC Symposium on Computer Systems in Safety-Critical Applications (SAFECOMP'92)*, pages 203–208, Zürich, Switzerland, October 1992.

[130] Ulrich Schmid and Wolfgang Kastner. Monitoring of distributed real-time systems: The Versatile Timing Analyzer (VTA). In *Proceedings Workshop on Performance Measurement and Visualization of Parallel Systems*, pages 277–302, Moravany/CSFR (October 1992), 1993. (Preliminary version of [39]).

[131] Ulrich Schmid. Monitoring of distributed real-time systems. In *Proceedings NATO ASI on Real-Time Computing*, pages 582–583, Sint Maarten, October 1994. (Appeared as Wolfgang A. Halang and Alexander D. Stoyenko (eds.): Real time computing, NATO ASI Series F: Computer and Systems Sciences, Vol. 127, 1994.).

[132] Ulrich Schmid. The role of standards in real-time computing. In *Proceedings NATO ASI on Real-Time Computing*, pages 638–639, Sint Maarten, October 1994. (Appeared as Wolfgang A. Halang and Alexander D. Stoyenko (eds.): Real time computing, NATO ASI Series F: Computer and Systems Sciences, Vol. 127, 1994.).

[133] Ulrich Schmid. Monitoring in verteilten Echtzeitsystemen. In *Proceedings Echtzeit'91*, pages 169–176, Sindelfingen, Germany, June 1991.

[134] Ulrich Schmid. The average CRI-length of a tree collision resolution algorithm in presence of multiplicity-dependent capture effects. In *Proceedings 19th International Colloquium on Automata, Languages, and Programming (ICALP'92)*, pages 223–234, Vienna, Austria, July 1992. (Appeared as Lecture Notes on Computer Science 623, Springer-Verlag, 1992).

[135] Johann Blieberger, Gerhard-Helge Schildt, Ulrich Schmid, and Stefan Stöckler. *Informatik*. Springer-Verlag, Vienna, Austria, 1.(1990), 2.(1992) edition, 1990.

[136] Bernadette Charron-Bost, Shlomi Dolev, Jo Ebergen, and Ulrich Schmid. 08371 summary – fault-tolerant distributed algorithms on vlsi chips. In Bernadette Charron-Bost, Shlomi Dolev, Jo Ebergen, and Ulrich Schmid, editors, *Fault-Tolerant Distributed Algorithms on VLSI Chips*, number 08371 in Dagstuhl Seminar Proceedings, Dagstuhl, Germany, 2009. Schloss Dagstuhl - Leibniz-Zentrum fuer Informatik, Germany. http://drops.dagstuhl.de/opus/frontdoor.php?source_opus=1927.

[137] Ulrich Schmid, editor. *Special Issue on The Challenge of Global Time in Large-Scale Distributed Real-Time Systems*, J. Real-Time Systems 12(1–3), 1997.

[138] M. Schwarz, M. Zeiner, and U. Schmid. Linear-Time Data Dissemination in Dynamic Networks. ArXiv e-prints: https://arxiv.org/abs/1701.06800, January 2017.

[139] Laurent Prosperi, Roman Kuznets, and Ulrich Schmid. Knowlege in byzantine message-passing systems. Technical Report TUW-260549, E185 - Institut für Computersprachen, E182 - Institut für Technische Informatik; Technische Universität Wien, 2017. http://publik.tuwien.ac.at/files/PubDat_260549.pdf.

[140] Kyrill Winkler, Manfred Schwarz, and Ulrich Schmid. Consensus in directed dynamic networks with short-lived stability. *CoRR*, abs/1602.05852, 2016. (submitted).

[141] Martin Zeiner, Ulrich Schmid, Udo Schilcher, and Christian Bettstetter. FWF-proposal SPRG: Structural properties of random graphs. Research Report TUW-544205, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 1-3/182-2, 1040 Vienna, Austria, 2016. http://publik.tuwien.ac.at/files/PubDat_544205.pdf.

[142] Danny Dolev, Matthias Függer, Christoph Lenzen, Martin Perner, and Ulrich Schmid. Hex: Scaling honeycombs is easier than scaling clock trees, 2015. (submitted to JCSS).

[143] Daniel Pfleger and Ulrich Schmid. A framework for connectivity monitoring in wireless sensor networks. Research Report TUW-241107, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 1-3/182-2, 1040 Vienna, Austria, 2015. http://publik.tuwien.ac.at/files/PubDat_241107.pdf (appeared in Proc. IARIA SENSORCOMM'16, Nice, France, 2016).

[144] Ulrich Schmid. Final report FWF FATAL-project (P21694). Research Report TUW-235380, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 1-3/182-2, 1040 Vienna, Austria, 2013. http://publik.tuwien.ac.at/files/PubDat_235380.pdf.

[145] Ulrich Schmid. FWF-proposal ADynNet: Gracefully degrading agreement in directed dynamic networks. Research Report TUW-235381, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 1-3/182-2, 1040 Vienna, Austria, 2014. http://publik.tuwien.ac.at/files/PubDat_235381.pdf.

[146] Martin Biely, Peter Robinson, Ulrich Schmid, and Kyrill Winkler. Impossibility results for k-set agreement in message-passing systems, 2014. (submitted to Information & Computation).

[147] Matthias Függer, Robert Najvirt, Thomas Nowak, and Ulrich Schmid. Faithful glitch propagation in binary circuit models. *arXiv:1406.2544*, 2014. (an extended abstract appeared in Proc. DATE'15).

[148] Manfred Schwarz, Kyrill Winkler, Ulrich Schmid, Martin Biely, and Peter Robinson. Gracefully degrading consensus and k-set agreement under dynamic link failures. Research Report TUW-220473, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 1-3/182-2, 1040 Vienna, Austria, 2013. http://publik.tuwien.ac.at/files/PubDat_220473.pdf.

[149] Ulrich Schmid. Final report FWF PSRTS-project (P20529). Research Report TUW-235379, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 1-3/182-2, 1040 Vienna, Austria, 2013. http://publik.tuwien.ac.at/files/PubDat_235379.pdf.

[150] Martin Biely, Peter Robinson, and Ulrich Schmid. Agreement in directed dynamic networks. *arXiv:1204.0641*, April 2012.

[151] Matthias Függer and Ulrich Schmid. FWF-proposal SIC: Self-stabilizing Byzantine fault-tolerant distributed algorithms for integrated circuits. Research Report 60/2012, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 1-3/182-1, 1040 Vienna, Austria, 2012.

[152] Andreas Steininger, Ulrich Schmid, and Horst Zimmermann. Fwf-proposal EASET: Accelerator-based experimental analysis and simulation modeling of single-event transients in VLSI circuits. Research Report 61/2012, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 1-3/182-1, 1040 Vienna, Austria, 2012.

[153] Martin Biely, Peter Robinson, and Ulrich Schmid. Just enough synchrony for message-passing k-set agreement. Research Report 6/2010, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 1-3/182-1, 1040 Vienna, Austria, 2010.

[154] Martin Biely, Peter Robinson, and Ulrich Schmid. Solving k-set agreement with stable skeleton graphs. Research Report 28/2010, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 1-3/182-1, 1040 Vienna, Austria, 2010.

[155] Andreas Dielacher, Matthias Fuegger, and Ulrich Schmid. How to speed-up fault-tolerant clock generation in VLSI systems-on-chip via pipelining. Research Report 15/2009, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 1-3/182-1, 1040 Vienna, Austria, 2009. http://www.vmars.tuwien.ac.at/documents/extern/2571/techreport.pdf.

[156] Matthias Fuegger and Ulrich Schmid. Fault-tolerant distributed tick generation in VLSI systems-on-chip. Research Report 53/2009, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 1-3/182-2, 1040 Vienna, Austria, 2009.

[157] Martin Biely, Peter Robinson, and Ulrich Schmid. Weak synchrony models and failure detectors for message passing k-set agreement. Research Report 51/2009, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 1-3/182-2, 1040 Vienna, Austria, 2009.

[158] Ulrich Schmid, Andreas Steininger, and Horst Zimmermann. FWF-proposal FATAL: A modeling framework for fault-tolerant asynchronous logic. Research Report 70/2008, Technische Universität Wien, Institut für Technische Informatik, Treitlstrasse 1-3/182-1, 1040 Vienna, Austria, 2008.

[159] Ulrich Schmid. Final report FWF Theta-project (P17757-N04). Research Report 71/2008, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 1-3/182-1, 1040 Vienna, Austria, 2008.

[160] Ulrich Schmid. FWF project proposal: Partially synchronous distributed real-time systems (PSRTS). Research Report 48/2007, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 1-3/182-1, 1040 Vienna, Austria, 2007.

[161] Ulrich Schmid. Proposal Uni-Infrastruktur IV: Robust embedded systems. Research Report 84/2007, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 1-3/182-1, 1040 Vienna, Austria, 2007.

[162] Ulrich Schmid and Michael Drmota. WWTF project proposal: Mathematics and distributed computing. Research Report 83/2007, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 1-3/182-1, 1040 Vienna, Austria, 2007.

[163] Andreas Steininger, Ulrich Schmid, Matthias Fuegger, and Gottfried Fuchs. A fault-tolerant distributed algorithms perspective of systems-on-chip. Research Report 2/2007, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 1-3/182-1, 1040 Vienna, Austria, 2007.

[164] Matthias Fuegger, Ulrich Schmid, Gottfried Fuchs, and Gerald Kempf. Fault-Tolerant Distributed Clock Generation in VLSI Systems-on-Chip. Research Report 12/2006, Technische Universität Wien, Institut für Technische Informatik, 2006.

[165] Heinrich Moser and Ulrich Schmid. Optimal clock synchronization revisited: Upper and lower bounds in real-time systems. Research Report 71/2006, Vienna University of Technology, Institut für Technische Informatik, Treitlstr. 1-3/182-2, 1040 Vienna, Austria, 2006.

[166] Ulrich Schmid, Andreas Steininger, and Helmut Veith. Towards a systematic design of fault-tolerant asynchronous circuits. Research Report 98/2006, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 1-3/182-1, 1040 Vienna, Austria, 2006. (A short version appeared at Zuverlässigkeit und Design (ZuD'07)).

[167] Ulrich Schmid and Markus Proske. FIT-IT project proposal ProSCE: Promoting science in computer engineering. Research Report 125/2006, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 1-3/182-1, 1040 Vienna, Austria, 2006.

[168] Ulrich Schmid and Markus Proske. FIT-IT project proposal ESiA: Embedded systems in action. Research Report 1/2007, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 1-3/182-1, 1040 Vienna, Austria, 2007.

[169] Christof Fetzer and Ulrich Schmid. On the possibility of consensus in asynchronous systems with finite average response times. Research Report 14/2004, Technische Universität Wien, Institut für Technische Informatik, Treitlstraße 3, A-1040 Vienna, Austria, 2004. (Brief announcement appeared at PODC'04).

[170] Ulrich Schmid. Final report START-project Y41. Research Report 19/2004, Technische Universität Wien, Institut für Technische Informatik, Treitlstraße 3, A-1040 Vienna, Austria, 2004.

[171] Ulrich Schmid and Andreas Steininger. Dezentrale Fehlertolerante Taktgenerierung in VLSI Chips. Research Report 69/2004, Technische Universität Wien, Institut für Technische Informatik, 2004. International patent PCT WO2006/007619: EP 1769356, US 2009/0102534, ZL 200580024166.6, AT 501510.

[172] Gottfried Fuchs, Ulrich Schmid, and Andreas Steininger. Ein Verfahren für das verteilte Generieren eines fehlertoleranten adaptiven Taktes in Hardware. Research Report 18/2004, Technische Universität Wien, Institut für Technische Informatik, 2004.

[173] Ulrich Schmid and Bettina Weiss. FWF project proposal: Fault-tolerant distributed algorithms in sparse ad hoc wireless networks. Research Report 13/2004, Vienna University of Technology, Institut für Technische Informatik, Treitlstr. 1-3/182-2, 1040 Vienna, Austria, 2004.

[174] Bernd Thallner and Ulrich Schmid. Distributed construction of sparse fault-tolerant overlay networks. Research Report 35/2004, Technische Universität Wien, Institut für Technische Informatik, Treitlstraße 3, A-1040 Vienna, Austria, 2004. (submitted).

[175] Ulrich Schmid. Failure model coverage under transient link failures. Research Report 2/2004, Technische Universität Wien, Institut für Technische Informatik, Treitlstraße 3, A-1040 Vienna, Austria, 2004. (submitted).

[176] Ulrich Schmid and Bettina Weiss. Synchronous Byzantine agreement under hybrid process and link failures. Research Report 1/2004, Technische Universität Wien, Institut für Technische Informatik, Treitlstraße 3, A-1040 Vienna, Austria, 2004. (submitted).

[177] Gérard Le Lann and Ulrich Schmid. How to implement a timer-free perfect failure detector in partially synchronous systems. Technical Report 183/1-127, Department of Automation, Technische Universität Wien, January 2003. (Replaced by Research Report 28/2005, Institut für Technische Informatik, TU Wien, 2005.).

[178] Gérard Le Lann and Ulrich Schmid. How to maximize computing systems coverage. Technical Report 183/1-128, Department of Automation, Technische Universität Wien, April 2003.

[179] Ulrich Schmid. FWF project proposal: Asynchronous distributed algorithms in the Theta-model. Technical Report 183/1-133, Department of Automation, TU Vienna, December 2003.

[180] Ulrich Schmid and Johann Vilanek. FIT-IT project proposal: Seamless campus. Technical Report 183/1-136, Department of Automation, TU Vienna, December 2003.

[181] Bernd Thallner and Ulrich Schmid. Fault tolerant communication topologies for wireless ad hoc networks. Technical Report 183/1-132, Department of Automation, TU Vienna, December 2003.

[182] Josef Widder, Gérard Le Lann, and Ulrich Schmid. Perfect failure detection with booting in partially synchronous systems. Technical Report 183/1-131, Department of Automation, Technische Universität Wien, April 2003. (preliminary version of [99]).

[183] Ulrich Schmid and Bettina Weiss. Synchronous Byzantine agreement under hybrid process and link failures. Technical Report 183/1-124, Department of Automation, Technische Universität Wien, November 2002. (replaces TR 183/1-110).

[184] Ulrich Schmid and Christof Fetzer. Randomized asynchronous consensus with imperfect communications. Technical Report 183/1-120, Department of Automation, Technische Universität Wien, January 2002. (Extended version of [103]).

[185] Günther Gridling, Martin Hutle, Ulrich Schmid, Hannes Stratil, Bernd Thallner, and Bettina Weiss. Service specification of W2F. Technical Report 183/1-113, Department of Automation, Technische Universität Wien, 2001. (unfinished).

[186] Bettina Weiss and Ulrich Schmid. Consensus with written messages under link faults. Technical Report 183/1-114, Department of Automation, Technische Universität Wien, March 2001. (extended version of [106]).

[187] Ulrich Schmid, Martin Horauer, and Nikolaus Kerö. Hochgenaue Uhrensynchronisation in verteilten Systemen. Technical Report 183/1-117, Department of Automation, TU Vienna, October 2001.

[188] Ulrich Schmid and Robert Sablatnig. EDV-Pflichtlaborkonzept Informatik. Technical Report 183/1-118, Vienna University of Technology, Department of Automation, October 2001.

[189] Ulrich Schmid. Bakkalaureats- und Magisterstudium Technische Informatik. Technical Report 183/1-119, Vienna University of Technology, Department of Automation, October 2001.

[190] Ulrich Schmid and Bettina Weiss. Consensus with oral/written messages: Link faults revisited. Technical Report 183/1-110, Department of Automation, Technische Universität Wien, February 2001. (obsolete, replaced by TR 183/1-124).

[191] Martin Biely and Ulrich Schmid. Message-efficient consensus in presence of hybrid node and link faults. Technical Report 183/1-116, Department of Automation, Technische Universität Wien, August 2001.

[192] Ulrich Schmid. Report on 3 years of START-project Y41-MAT. Technical Report 183/1-100, Department of Automation, Technische Universität Wien, February 2000.

[193] Nikolaus Kerö, Ulrich Schmid, and Martin Horauer. Verfahren für die Synchronisation von Computeruhren in Netzwerken. Technical Report 183/1-105, Department of Automation, TU Vienna, March 2000. Austrian Gebrauchsmuster AT005327U1 (2002); Europe and Japan patents pending.

[194] Ulrich Schmid, Wolfgang Kastner, Bernd Burgstaller, and Christian Kral. Skriptum zur Laborübung Prozeßautomatisierung. Technical Report 183/1-106-a, Vienna University of Technology, Department of Automation, June 2000.

[195] Ulrich Schmid. Verteilte Embedded Systems unter OSE. Technical Report 183/1-107, Department of Automation, TU Vienna, June 2000.

[196] Ulrich Schmid. A perception-based fault model for single-round agreement algorithms. Technical Report 183/1-108, Technische Universität Wien, Department of Automation, October 2000.

[197] Ulrich Schmid and Thomas Mandl. Implementation of the NTI Device-Handler. Technical Report 183/1-86, Technische Universität Wien, Department of Automation, January 1999.

[198] Thomas Mandl, Herbert Nachtnebel, and Ulrich Schmid. Network Time Interface user manual. Technical Report 183/1-87, Technische Universität Wien, Department of Automation, January 1999. (in German).

[199] Gerda Richter, Michael Schmidt, and Ulrich Schmid. i82596 NTI Device-Driver software documentation. Technical Report 183/1-90, Technische Universität Wien, Department of Automation, February 1999.

[200] Ulrich Schmid. Basic features of the wireline/wireless factory/facility fieldbus. Technical Report 183/1-95, Department of Automation, Technische Universität Wien, August 1999.

[201] Martina Umlauft and Ulrich Schmid. GPS Device-Driver software documentation. Technical Report 183/1-97, Technische Universität Wien, Department of Automation, October 1999.

[202] Ulrich Schmid. Lehrbedarfs- und Lehrkapazitätserhebung für die Technisch-Naturwissenschaftlichen Fakultät der TU-Wien. Technical Report 183/1-98, Vienna University of Technology, Department of Automation, October 1999.

[203] Ulrich Schmid. Stellenbewirtschaftungsmodell für die Fakultät TNF und die Fachgruppe Informatik. Technical Report 183/1-82, Vienna University of Technology, Department of Automation, February 1998.

[204] Christian Kral, Thomas Mandl, Ulrich Schmid, and Klaus Schossmaier. Tips für die Messe-Präsentation von Forschungsergebnissen. Technical Report 183/1-83, Technische Universität Wien, Department of Automation, April 1998. (in German).

[205] Silvia Miksch, Ulrich Schmid, Martin Schönhacker, Katrin Seyr, and Martina Umlauft. Evaluierung der Informatik. Technical Report 183/1-84, Vienna University of Technology, Department of Automation, November 1998. (Also appeared as Institutsbericht Nr. 38, Institut für Computergraphik, Abteilung für Algorithmen und Programmiermethodik, Technische Universität Wien, November 1998.).

[206] Ulrich Schmid, Winfried Auzinger, Robert Sablatnig, Karlheinz Schwarz, Herbert Störi, and Bruno Wöhrer. EDV-Laborkonzept für die Fakultät TNF. Technical Report 183/1-85, Vienna University of Technology, Department of Automation, December 1998.

[207] Ulrich Schmid and Klaus Schossmaier. Interval-based clock synchronization revisited. Technical Report 183/1-80, Technische Universität Wien, Department of Automation, July 1997.

[208] Ulrich Schmid. Kabel-Fehlerortung mit SynUTC. Technical Report 183/1-81, Technische Universität Wien, Department of Automation, July 1997. (Patent: German Gebrauchsmuster 296 23086.3).

[209] Ulrich Schmid. Application to START. Technical Report 183/1-65, Vienna University of Technology, Department of Automation, January 1996.

[210] Ulrich Schmid. Static priority scheduling of aperiodic real-time tasks. Technical Report 183/1-47, Vienna University of Technology, Department of Automation, May 1994. (Extension of [35]).

[211] Martin Horauer, Dietmar Loy, and Ulrich Schmid. NTI functional and architectural specification. Technical Report 183/1-69, Technische Universität Wien, Department of Automation, December 1996. (revised 1998).

[212] Klaus Schossmaier and Ulrich Schmid. UTCSU functional specification. Technical Report 183/1-56, Technische Universität Wien, Department of Automation, July 1995.

[213] Ulrich Schmid and Werner Staringer. Geschichte des Informatik-Labors Treitlstraße 3, 1. Stock. Technical Report 183/1-57, Vienna University of Technology, Department of Automation, July 1995.

[214] Ulrich Schmid, Dietmar Loy, and Wolfgang Kastner. Project proposal SSCMP: Sequenced Synchronized Clock Multicast Protocol. Technical Report 183/1-58, Vienna University of Technology, Department of Automation, August 1995.

[215] Ulrich Schmid. An annotated bibliography on clock synchronization in distributed systems. Technical Report 183/1-45, Technische Universität Wien, Department of Automation, December 1994. (incomplete).

[216] Ulrich Schmid and Dietmar Loy. FWF-Projektantrag SynUTC — Synchronized UTC for distributed real-time systems. Technical Report 183/1-39, Technische Universität Wien, Department of Automation, December 1993.

[217] Ulrich Schmid. Zusatzantrag zum FWF-Projekt VTA. Technical Report 183/1-36, Vienna University of Technology, Department of Automation, April 1993.

[218] Ulrich Schmid and Wolfgang Kastner. DOBOS - Konzept eines distributed object-based operating systems. Technical Report 183/1-40, Vienna University of Technology, Department of Automation, December 1993. (Extension of [123]).

[219] Ulrich Schmid. Determining the size of dedicated shared memory areas for client-server applications. Technical Report 183/1-44, Vienna University of Technology, Department of Automation, August 1993.

[220] Thomas Hontsch and Ulrich Schmid. Instrumentierung auf Sourcecode-Level. Technical Report 183/1-26, Vienna University of Technology, Department of Automation, January 1992.

[221] Michael Drmota and Ulrich Schmid. The analysis of the expected successful operation time of slotted ALOHA. Technical Report 183/1-33, Vienna University of Technology, Department of Automation, December 1992. (Extension of [41]).

[222] Johann Blieberger and Ulrich Schmid. Qualifying dynamic task scheduling in hard real-time systems: A novel approach. Technical Report 183/1-15, Vienna University of Technology, Department of Automation, January 1991.

[223] Ulrich Schmid. The average CRI-length of a tree collision resolution algorithm in presence of multiplicity-dependent capture effects. Technical Report 183/1-19, Vienna University of Technology, Department of Automation, May 1991. (Extension of [134]).

[224] Ulrich Schmid and Stefan Stöckler. Konzept der Laborübung Prozeßautomatisierung. Technical Report 183/1-21, Vienna University of Technology, Department of Automation, June 1991.

[225] Ulrich Schmid. FWF-Projektantrag Versatile Timing Analyzer (VTA). Technical Report 183/1-22, Vienna University of Technology, Department of Automation, June 1991.

[226] Ulrich Schmid. Das Workstation-LAN der Abteilung Automatisierungssysteme. Technical Report 183/1-25, Vienna University of Technology, Department of Automation, October 1991.

[227] Ulrich Schmid. Easy impossibility proofs for k-set agreement. In Dmitry Feichtner-Kozlov and Damien Imbs, editors, *Report Dagstuhl-Seminar 16282 Topological Methods in Distributed Computing*, volume 6(7), page 39, Dagstuhl, Germany, 2016. Schloss Dagstuhl–Leibniz-Zentrum fuer Informatik.

[228] Danny Dolev, Matthias Függer, Christoph Lenzen, Ulrich Schmid, and Andreas Steininger. Fault-tolerant distributed systems in hardware. *Bulletin of EATCS*, 2(116):112–153, 2015.

[229] Annu Gmeiner, Igor Konnov, Ulrich Schmid, Helmut Veith, and Josef Widder. Tutorial on parameterized model checking of fault-tolerant distributed algorithms. In *Formal Methods for Executable Software Models - 14th International School on Formal Methods for the Design of Computer, Communication, and Software Systems (SFM'14), 2014, Bertinoro, Italy, June 16-20, 2014, Advanced Lectures*, pages 122–171, 2014.

[230] Michael Hofbauer, Kurt Schweiger, Horst Dietrich Wolfgang Gaberl, Horst Zimmermann, Ulrich Giesen, Frank Langer, Ulrich Schmid, and Andreas Steininger. Single event transient pulse shape measurements by on-chip sense amplifiers in a single inverter for intermediate input states under alpha irradiation, 2013. Poster at IEEE Nuclear and Space Radiation Effects Conference (NSREC'13).

[231] Danny Dolev, Matthias Fuegger, Christoph Lenzen, and Ulrich Schmid. Towards self-stabilizing byzantine fault-tolerant clock generation in systems-on-chip. In *2012 NITRD National Workshop on the New Clockwork for Time-Critical Systems, October 25-26, Baltimore (USA)*, Oct. 2012.

[232] Michael Hofbauer, Kurt Schweiger, Horst Dietrich, Horst Zimmermann, Ulrich Schmid, and Bruno Merk. Single event effect measurements in 90nm CMOS circuits at the microbeam facility for the project FATAL. In *GSI Scientific Report 2011*, page 424, GSI Helmholtzzentrum für Schwerionenforschung GmbH, Darmstadt, Germany, 2012.

[233] Michael Hofbauer, Kurt Schweiger, Horst Zimmermann, and Ulrich Schmid. Projekt FATAL, 2012. Vienna Scientific Cluster Brochure 2012, p. 53.

[234] Michael Hofbauer, Kurt Schweiger, Horst Zimmermann, Ulrich Giesen, Frank Langner, Ulrich Schmid, and Andreas Steininger. Supply voltage dependent on-chip single event transient pulse shape measurements in 90 nm bulk CMOS under alpha irradiation. In *Proceedings 21st European Conference on Radiation and its Effects on Components and Systems (RADECS'12)*, Sep. 2012.

[235] Michael Hofbauer, Kurt Schweiger, Horst Dietrich, Horst Zimmermann, Kay-Obbe Voss, Bruno Merk, Ulrich Schmid, and Andreas Steininger. Pulse shape measurements by on-chip sense amplifiers of single event transients propagating through a 90 nm bulk CMOS inverter chain, 2012. Poster at IEEE Nuclear and Space Radiation Effects Conference (NSREC'12), Miami (USA).

[236] Michael Hofbauer, Kurt Schweiger, Horst Dietrich, Horst Zimmermann, Ulrich Schmid, and Ulrich Giesen. Messung der Auswirkungen von ionisierender Strahlung auf 90 nm CMOS Schaltungen. Technical report, Physikalisch Technische Bundesanstalt, 2012.

[237] Heinrich Moser and Ulrich Schmid. Construction of a fault-tolerant wireless communication topology using distributed agreement. In *Proceedings of the Junior Scientist Conference 2006*, pages 47–48, Vienna, Austria, Apr. 2006.

[238] Gérard Le Lann and Ulrich Schmid. Proof-based systems engineering in assert. In *Proceedings Data Systems in Aerospace (DASIA'05)*, Edinburgh, Scotland, May–June 2005.

[239] Wolfgang Hawlik. Aus Spaß an Neuem. *Computer Kommunikativ*, 4, 2002. (Portrait anläßlich Berufung U. Schmid).

[240] Margit Schwarz, editor. *START und Wittgenstein 1996–2000*. Austrian Federal Ministry of Education, Science and Culture and Austrian Science Fund, 2001. (START-Price U. Schmid, 1996).

[241] Michael Freund and Ulrich Schmid. *In fehlertoleranten Computernetzwerken*, pages 57–59. Springer Verlag, 1997.

[242] Ulrich Schmid. Challenges in interval-based clock synchronization. In *Seminar-Report 185 of Dagstuhl-Seminar 9728 on "Average Case Analysis of Algorithms"*, pages 19–20, Schloß Dagstuhl, Germany, July 7–11, 1997.

[243] Ulrich Schmid. Interval-based clock synchronization. In *Seminar-Report 138 of Dagstuhl-Seminar 9611 on "Time Services"*, page 7, Schloß Dagstuhl, Germany, March 1996. (Reprinted in Real-Time Systems 12(3):334, 1997).

[244] Ulrich Schmid. ECCS-related research activities at the department of automation, Technische Universität Wien, 1994. In *Newsletter IEEE Technical Segment Committee on Engineering of Complex Computer Systems (ECCS)*, 1(2) Part A, 1994, pages 2–5.

[245] Ulrich Schmid. On random-trees arising in the analysis of scheduling algorithms for real-time systems. In *Seminar-Report 68 of Dagstuhl-Seminar 9328 on "Average Case Analysis of Algorithms"*, page 15, Schloß Dagstuhl, Germany, July 1993.

[246] Ulrich Schmid. *Analyse von Collision Resolution Algorithmen in Random-Access Systemen mit dominanten Übertragungskanälen.* PhD thesis, Technische Universität Wien, Faculty of Technical and Natural Sciences, Department of Algebra und Discrete Mathematics, 1986.

[247] Ulrich Schmid. Abzählmethoden der Theoretischen Informatik. Master's thesis, Technische Universität Wien, Department of Algebra und Discrete Mathematics, 1985.

[248] Alexander Kößler. *Real-Time Performance Analysis of Synchronous Distributed Systems.* PhD thesis, Technische Universität Wien, Fakultät für Informatik, 2014.

[249] Peter Robinson. *Weak System Models for Fault-Tolerant Distributed Agreement Problems.* PhD thesis, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 3/3/182-1, 1040 Vienna, Austria, 2011.

[250] Matthias Függer. *Analysis of On-Chip Fault-Tolerant Distributed Algorithms.* PhD thesis, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 3/3/182-2, 1040 Vienna, Austria, 2010.

[251] Heinrich Moser. *A Model for Distributed Computing in Real-Time Systems.* PhD thesis, Technische Universität Wien, Fakultät für Informatik, May 2009. (Promotion sub auspiciis).

[252] Martin Biely. *Dynamic Aspects of Modeling Distributed Computations.* PhD thesis, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 3/3/182-1, 1040 Vienna, Austria, 2009.

[253] Hannes Stratil. *Advantages and Limitations of Position-based Communication in Wireless Ad-hoc Networks.* PhD thesis, Technische Universität Wien, Fakultät für Informatik, 2006. Published as H. Stratil: The usage of planar graphs in wireless ad-hoc networks, Südwestdeutscher Verlag für Hochschulschriften, ISBN 3838102789, 2009.

[254] Bernd Thallner. *Topology Control for Fault-Tolerant Communication in Wireless Ad Hoc Networks.* PhD thesis, Embedded Computing Systems Group, Vienna University of Technology, April 2005. http://www.ecs.tuwien.ac.at/W2F/documents/diss_thallner.pdf.

[255] Martin Hutle. *Failure Detection in Sparse Networks.* PhD thesis, Vienna University of Technology, 2005.

[256] Martin Horauer. *Clock Synchronization in Distributed Systems.* PhD thesis, Vienna University of Technology, Fakultät für Elektrotechnik, February 2004.

[257] Josef Widder. *Distributed Computing in the Presence of Bounded Asynchrony.* PhD thesis, Vienna University of Technology, Fakultät für Informatik, May 2004.

[258] Bettina Weiss. *Authenticated Consensus.* PhD thesis, Technische Universität Wien, Fakultät für Technische Naturwissenschaften und Informatik, October 2002.

[259] Dieter Höchtl. *Atomic Multicasting in SSCMP.* PhD thesis, Technische Universität Wien, Fakultät für Technische Naturwissenschaften und Informatik, 1999. (Unfinished; Dieter died unforseen in 1999.).

[260] Klaus Schossmaier. *Interval-based Clock State and Rate Synchronization.* Dissertation, Technische Universität Wien, Fakultät für Technische Naturwissenschaften und Informatik, 1998. (Appeared in Dissertationen der Technischen Universität Wien, Band 87. Österreichischer Kunst- und Kulturverlag, Wien, 2000, ISBN 3-85437-201-9.).

[261] Dietmar Loy. *GPS-Linked High Accuracy NTP Time Processor for Distributed Fault-Tolerant Real-Time Systems.* Dissertation, Vienna University of Technology, Fakultät für Elektrotechnik, April 1996. (Appeared in Dissertationen der Technischen Universität Wien, Band 78. Österreichischer Kunst- und Kulturverlag, Wien 1997, ISBN 3-85437-056-3).

[262] Stefan Stöckler. *Event-based monitoring of distributed real-time systems.* PhD thesis, Technische Universität Wien, Fakultät für Technische Naturwissenschaften und Informatik, 1994.

[263] Kyrill Winkler. Easy impossibility proofs for k-set agreement. Master's thesis, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 3/2/182-2, 1040 Vienna, Austria, 2013.

[264] Manfred Schwarz. Solving k-set agreement in dynamic networks. Master's thesis, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 3/2/182-2, 1040 Vienna, Austria, 2013.

[265] Martin Perner. Self-stabilizing byzantine fault-tolerant clock distribution in grids. Master's thesis, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 3/2/182-2, 1040 Vienna, Austria, 2013.

[266] Markus Hofstätter. Solving the labeling problem: A byzantine fault-tolerant self-stabilizing FPGA prototype based on the FATAL$^+$ protocol. Master's thesis, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 3/2/182-2, 1040 Vienna, Austria, 2013.

[267] Markus Posch. Selbststabilisierende Byzantinisch fehlertolerante takterzeugung in FPGAs. Master's thesis, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 3/3/182-1, 1040 Vienna, Austria, 2012.

[268] Andreas Dielacher. A pipelined distributed fault-tolerant clock generation algorithm in VLSI - Proofs and implementation. Master's thesis, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 3/3/182-1, 1040 Vienna, Austria, 2010.

[269] Thomas Nowak. Topology in distributed computing. Master thesis, Embedded Computing Systems Group, Technische Universität Wien, March 2010.

[270] Matthias Függer. Fault-Tolerant Distributed Clock Generation in VLSI Systems-on-Chip. Master's thesis, Technische Universität Wien, Institut für Technische Informatik, Treitlstrasse 1-3/182-1, A-1040 Vienna, Austria, April 2006.

[271] Heinrich Moser. Distributed construction of a fault-tolerant wireless communication topology for networked embedded systems. Master's thesis, Embedded Computing Systems Group, Vienna University of Technology, February 2005.

[272] Daniel Albeseder. Experimentelle Verifikation von Synchronitätsannahmen für Computernetzwerke. Diplomarbeit, Embedded Computing Systems Group, Technische Universität Wien, May 2004. (in German).

[273] Martin Biely. Byzantine agreement under the perception-based fault model. Diplomarbeit, Technische Universität Wien, Department of Automation, February 2002.

[274] Hannes Stratil. Topology management and routing in wireless networks - an overview. Diplomarbeit, Technische Universität Wien, Department of Automation, February 2002.

[275] Josef Widder. Switching On. How processes initialize for consistent broadcast. Diplomarbeit, Technische Universität Wien, Department of Automation, October 2002.

[276] Albrecht Kadlec. Portierung des Betriebssystems pSOS^{+m} auf die AcQ i6040 Multiprozessor-CPU. Diplomarbeit, Technische Universität Wien, Department of Automation, 2000.

[277] Michael Kuen. Ein Multi-Master Interprozessor Bus. Diplomarbeit, Technische Universität Wien, Department of Automation, December 2000.

[278] Thomas Mandl. Network Time Interface Benutzerhandbuch. Diplomarbeit, Technische Universität Wien, Department of Automation, February 1999. (in German).

[279] Gerda Richter. Device driver for real-time communications coprocessor. Diplomarbeit, Technische Universität Wien, Department of Automation, June 1997.

[280] Bettina Weiss. Simulation environment for clock synchronization. Diplomarbeit, Technische Universität Wien, Department of Automation, June 1997.

[281] Dieter Höchtl. Verfügbarkeitsuntersuchung von GPS-Satellitenempfängern. Diplomarbeit, Technische Universität Wien, Department of Automation, September 1996.

[282] Fred-Frowin Fajtak. Objektorientierte Spezifikation graphischer Benutzerschnittstellen. Diplomarbeit, Technische Universität Wien, Department of Automation, 1996.

[283] Alfred Pusterhofer. NTSU Network Timestamp Unit: Ein Modul für Eventtimestamping und Uhrensynchronisation via LAN. Diplomarbeit, Technische Universität Wien, Department of Automation, May 1995. (in German).

[284] Roland Labner. Untersuchung über die Einsetzbarkeit graphischer Programmiermethoden für die On-Line Data Acquisition. Diplomarbeit, Technische Universität Wien, Department of Automation, 1994.

[285] Johann Divisch. Monitoring in verteilten Echtzeitsystemen: Objektorientiertes Schnittstellendesign. Diplomarbeit, Technische Universität Wien, Department of Automation, 1994.

[286] Johann Klasek. Dynamische Software- und Hardware-Instrumentierung. Diplomarbeit, Technische Universität Wien, Department of Automation, 1994.

[287] Martin Horauer. Entwicklung einer Network Timestamp Unit für einen Versatile Timing Analyzer zum Monitoring von verteilten Echtzeitsystemen. Diplomarbeit, Vienna University of Technology, Dept. of Computer Technology, Faculty of Electrical Engineering, September 1994. (in German).

[288] Werner Kastanek. Externe Prozeßsynchronisation im Betriebssystem REMUX. Diplomarbeit, Technische Universität Wien, Department of Automation, 1992.

[289] Thomas Hontsch. Sourcecode-Level Monitoring verteilter Echtzeitsysteme. Diplomarbeit, Technische Universität Wien, Department of Automation, 1991.

[290] Ulrich Schmid. Keynote: A perspective of fault-tolerant clock synchronization. In *IEEE Symposium on Precision Clock Synchronization for Measurement, Control and Communication (ISPCS'07)*, Vienna, Austria, October 1-3 2007.

[291] Martin Biely, Peter Robinson, and Ulrich Schmid. The generalized loneliness detector and weak system models for k-set agreement. *IEEE Transactions on Parallel and Distributed Systems*, 25(4):1078–1088, April 2014.

[292] Ulrich Schmid. Reconciling fault-tolerance and robustness ? Workshop on Design and Analysis of Robust Systems at CPS-Week 2016, Vienna, Austria, April 11 2016. (http://publik.tuwien.ac.at/files/publik_255368.pdf).

[293] Bernadette Charron-Bost, Shlomi Dolev, Jo Ebergen, and Ulrich Schmid, editors. *Fault-Tolerant Distributed Algorithms on VLSI Chips*, Schloss Dagstuhl, Germany, September 2008 2009. http://drops.dagstuhl.de/opus/frontdoor.php?source_opus=1927.

[294] Thomas Nowak, Matthias Függer, and Alexander Kößler. On the performance of a retransmission-based synchronizer. In *18th International Colloquium on Structural Information and Communication Complexity (SIROCCO)*, LNCS, 2011.

[295] Matthias Függer, Alexander Kößler, Thomas Nowak, and Martin Zeiner. Brief announcement: The degrading effect of forgetting on a synchronizer. In Andrea W. Richa and Christian Scheideler, editors, *Stabilization, Safety, and Security of Distributed Systems*, volume 7596 of *Lecture Notes in Computer Science*, pages 90–91. Springer Berlin Heidelberg, 2012.

[296] Gottfried Fuchs, Matthias Fuegger, and Andreas Steininger. On the threat of metastability in an asynchronous fault-tolerant clock generation scheme. In *15th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC'09)*, pages 127–136, Chapel Hill, N. Carolina, USA, May 2009.

[297] K. Schweiger, M. Hofbauer, H. Dietrich, H. Zimmermann, K.O. Voss, and B. Merk. Position dependent measurement of single event transient voltage pulse shapes under heavy ion irradiation. *Electronics Letters*, 48(3):171–172, 2012.

[298] Martin Hutle and Josef Widder. Self-stabilizing failure detector algorithms. In *Proc. IASTED International Conference on Parallel and Distributed Computing and Networks (PDCN'05)*, pages 485–490, Innsbruck, Austria, February 2005. IASTED/ACTA Press.

[299] Martin Hutle and Josef Widder. Brief announcement: On the possibility and the impossibility of message-driven self-stabilizing failure detection. In *Proceedings of the 24th ACM Symposium on Principles of Distributed Computing (PODC'05)*, page 208, Las Vegas, Nevada, USA, July 2005.

[300] Martin Hutle and Josef Widder. On the possibility and the impossibility of message-driven self-stabilizing failure detection. In *Proceedings of the Seventh International Symposium on Self Stabilizing Systems (SSS 2005)*, volume 3764 of *LNCS*, pages 153–170, Barcelona, Spain, October 2005. Springer Verlag.

[301] Daniel Albeseder. Evaluation of message delay correlation in distributed systems. In *Proceedings of the Third Workshop on Intelligent Solutions for Embedded Systems*, Hamburg, Germany, May 2005.

[302] Martin Biely and Josef Widder. Optimal message-driven implementations of omega with mute processes. *ACM Transactions on Autonomous and Adaptive Systems*, 4(1):Article 4, 22 pages, 2009.

[303] Heinrich Moser. Towards a real-time distributed computing model. *Theoretical Computer Science*, 410(6–7):629–659, Feb 2009.

[304] Martin Biely, Bernadette Charron-Bost, Antoine Gaillard, Martin Hutle, André Schiper, and Josef Widder. Tolerating corrupted communication. In *Proceedings of the 26th ACM Symposium on Principles of Distributed Computing (PODC'07)*, pages 244–253, Portland, OR, USA, August 2007. ACM.

[305] Bernadette Charron-Bost, Antoine Gaillard, Jennifer L. Welch, and Josef Widder. Routing without ordering. In *Proceedings 21st ACM Symposium on Parallelism in Algorithms and Architectures (SPAA'09)*, pages 145–153, 2009.

[306] Markus Ferringer, Gottfried Fuchs, Andreas Steininger, and Gerald Kempf. VLSI Implementation of a Fault-Tolerant Distributed Clock Generation. *IEEE International Symposium on Defect and Fault-Tolerance in VLSI Systems (DFT2006)*, pages 563–571, October 2006.

[307] Thomas Polzer, Thomas Handl, and Andreas Steininger. A metastability-free multi-synchronous communication scheme for fault-tolerant socs. Research Report 10/2009, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 1-3/182-1, 1040 Vienna, Austria, 2009.

[308] Gottfried Fuchs and Andreas Steininger. Vlsi implementation of a distributed algorithm for fault-tolerant clock generation. *Journal of Electrical and Computer Engineering*, 2011(936712), 2011.

[309] Ulrich Schmid and Bettina Weiss. Impossibility results and lower bounds for consensus under link failures. Technical Report 183/1-129, Department of Automation, Technische Universität Wien, April 2003. (submitted).

[310] Bernd Thallner, Heinrich Moser, and Ulrich Schmid. Topology control for fault-tolerant communication in wireless ad-hoc networks. Research Report 78/2005, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 1-3/182-1, 1040 Vienna, Austria, 2005. (preliminary version of [18]).

[311] Martin Hutle, Dahlia Malkhi, Ulrich Schmid, and Lidong Zhou. Chasing the weakest system model for implementing omega and consensus. Research Report 74/2005, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 1–3/182-2, 1040 Vienna, Austria, 2005. (appeared in IEEE TDSC 6(4):269-281, 2009.).

[312] Martin Biely, Ulrich Schmid, and Bettina Weiss. Synchronous consensus under hybrid process and link failures. Research Report 58/2009, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 1-3/182-2, 1040 Vienna, Austria, 2009.

[313] Bettina Weiss. Security in distributed systems - a survey. Technical Report 183/1-99, Department of Automation, Technische Universität Wien, February 2000.

[314] Bettina Weiss. Security issues in W2F. Technical Report 183/1-111, Department of Automation, Technische Universität Wien, July 2000.

[315] Günther Gridling. An algorithm for three-process consensus under restricted link failures. Technical Report 183/1-123, Department of Automation, Technische Universität Wien, October 2002.

[316] Günther Gridling. On the problem of internal interference in CDMA-based ad-hoc networks. Technical Report 183/1-121, Department of Automation, Technische Universität Wien, June 2002.

[317] Bettina Weiss. Authentication under denial-of-service attacks. In *Proc. IASTED International Conference on Communications and Computer Networks (CCN'02)*, pages 134–139, Boston, Massachusetts, USA, November 4–6, 2002.

[318] Bettina Weiss. Authentication under denial-of-service attacks. Technical Report 183/1-122, Department of Automation, Technische Universität Wien, July 2002.

[319] Bernd Thallner and Günther Gridling. Simulation of a wireless CDMA ad hoc network. In *Proc. IASTED International Conference on Communications and Computer Networks (CCN'02)*, pages 354–359, Boston, Massachusetts, USA, November 4–6, 2002.

[320] Josef Widder. Switching On: How to boot clock synchronization in partially synchronous systems. Technical Report 183/1-125, Department of Automation, Technische Universität Wien, December 2002. (Extended version of [323]).

[321] Martin Biely. Towards an optimal algorithm for hybrid Byzantine agreement. Technical Report 183/1-130, Department of Automation, Technische Universität Wien, April 2003. (Extended version of [322]).

[322] Martin Biely. An optimal Byzantine agreement algorithm with arbitrary node and link failures. In *Proc. 15th Annual IASTED International Conference on Parallel and Distributed Computing and Systems (PDCS'03)*, pages 146–151, Marina Del Rey, California, USA, November 3–5, 2003.

[323] Josef Widder. Booting clock synchronization in partially synchronous systems. In *Proceedings of the 17th International Symposium on Distributed Computing (DISC'03)*, volume 2848 of *LNCS*, pages 121–135, Sorrento, Italy, October 2003. Springer Verlag.

[324] Martin Hutle. An efficient failure detector for sparsely connected networks. In *Proc. IASTED International Conference on Parallel and Distributed Computing and Networks (PDCN'04)*, Innsbruck, Austria, February 2004.

[325] Martin Hutle. On omega in sparse networks. In *Proc. 10th International Symposium Pacific Rim Dependable Computing (PRDC'04)*, Papeete, Tahiti, March 2004.

[326] Bernd Thallner. Fault tolerant communication topologies for wireless ad hoc networks. In *Proceedings 1st Workshop on Dependability Issues in Wireless Ad Hoc Networks and Sensor Networks (DIWANS'04)*, pages 261–266, Florence, Italy, June 2004.

[327] Hannes Stratil. Design of a voronoi-aided routing (VAR) protocol for wireless sensor networks. Research Report 15/2004, Technische Universität Wien, Institut für Technische Informatik, Treitlstraße 3, A-1040 Vienna, Austria, 2004.

[328] Hannes Stratil. An efficient implementation of the greedy forwarding strategy. Research Report 16/2004, Technische Universität Wien, Institut für Technische Informatik, Treitlstraße 3, A-1040 Vienna, Austria, 2004. (submitted).

[329] Hannes Stratil. An efficient implementation of the greedy forwarding strategy. In *Proceedings of the Workshop on Sensor Networks*, pages 365–369, Ulm, Germany, September 2004.

[330] Hannes Stratil. Distributed construction of an underlay in wireless networks. In *Proceedings of the Second European Workshop on Wireless Sensor Networks*, pages 176–187, Istanbul, Turkey, January 2005.

[331] Heinrich Moser and Bernd Thallner. Distributed construction of fault-tolerant overlay networks: Construction algorithm. Research Report 39, Technische Universität Wien, Institut für Technische Informatik, July 2004.

[332] Bernd Thallner and Heinrich Moser. Topology control for fault-tolerant communication in highly dynamic wireless networks. In *Proceedings of the third International Workshop on Intelligent Solutions in Embedded Systems (WISES 2005)*, May 2005.

[333] Bernd Thallner and Heinrich Moser. Topology control for fault-tolerant communication in highly dynamic wireless networks. In *Proceedings of the Third Workshop on Intelligent Solutions for Embedded Systems (WISES 2005)*, May 2005.

[334] Hannes Stratil. Fault tolerant topology control with unreliable failure detectors. In *17th International Conference on Parallel and Distributed Computing and Systems*, November 14–16, 2005.

[335] Hannes Stratil. Voronoi supported communication in wireless ad-hoc networks. In *2nd International Symposium on Voronoi Diagrams in Science and Engineering*, October 10–13, 2005.

[336] Martin Biely. On the impact of link faults on Byzantine agreement. Research Report 48/2006, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 1-3/182-2, 1040 Vienna, Austria, 2006. (submitted).

[337] Heinrich Moser and Bernd Thallner. Construction of a fault-tolerant wireless communication topology using distributed agreement. In *DIWANS '06: Proceedings of the 2006 workshop on Dependability issues in wireless ad hoc networks and sensor networks*, pages 35–44, New York, NY, USA, 2006. ACM Press.

[338] Hannes Stratil and Ulrich Schmid. Efficient position-based communication in wireless ad-hoc networks. In *Proceedings of the Junior Scientist Conference 2006*, pages 75–76, Vienna, Austria, Apr. 2006.

[339] Josef Widder, Günther Gridling, Bettina Weiss, and Jean-Paul Blanquart. Synchronous consensus with mortal Byzantines. In *Proceedings of the International Conference on Dependable Systems and Networks (DSN'07)*, pages 102–111, Edinburgh, UK, June 2007.

[340] Martin Horauer and Dietmar Loy. Adder synthesis. In *Proceedings AUSTROCHIP'95*, Graz, Austria, 1995.

[341] Klaus Schossmaier and Dietmar Loy. An ASIC supporting external clock synchronization for distributed real-time systems. In *Proceedings of the 8th Euromicro Workshop on Real-Time Systems*, pages 277–282, L'Aquila, Italy, June 1996.

[342] Klaus Schossmaier. UTCSU — an ASIC to support clock synchronization for distributed real-time systems. In *Seminar-Report 138 of Dagstuhl-Seminar 9611 on "Time Services"*, page 8, Schloß Dagstuhl, Germany, March 1996. (Reprinted in Real-Time Systems 12(3), 1997, p. 334).

[343] Martin Horauer. A primer to digital design with Synopsys and Cadence. Technical Report 183/1-68, Technische Universität Wien, Department of Automation, October 1996.

[344] Klaus Schossmaier. Understanding interval-based clock rate synchronization algorithms. Technical Report 183/1-70, Technische Universität Wien, Department of Automation, December 1996.

[345] Martin Horauer and Dietmar Loy. UTCLIENT – an ASIC supporting clock synchronization in distributed real-time systems. In *Proceedings AUSTROCHIP'97*, pages 290–296, Linz, Austria, April 9, 1997.

[346] Klaus Schossmaier. An interval-based framework for clock rate synchronization algorithms. In *Proceedings 16th ACM Symposium on Principles of Distributed Computing*, pages 169–178, St. Barbara, USA, August 21–24, 1997.

[347] Dietmar Loy. Time-services hardware support in fault-tolerant real-time systems. In *Proceedings of the 5th International Conference on VLSI and CAD (ICVC'97)*, Seoul, Korea, October 13–15, 1997.

[348] Martin Horauer and Dietmar Loy. Hardware-unterstützte Uhrensynchronisation in Verteilten Systemen. In *Proceedings AUSTROCHIP'98*, pages 67–72, Wiener Neustadt, Austria, October 1998. (ISBN 3-901578-03-X, in German).

[349] Klaus Schossmaier and Bettina Weiss. An algorithm for fault-tolerant clock state & rate synchronization. In *Proceedings 18th IEEE Symposium on Reliable Distributed Systems (SRDS'99)*, pages 36–47, Lausanne, Switzerland, October 19–22, 1999.

[350] Bettina Weiss. Simulation environment for clock synchronization. Technical Report 183/1-88, Technische Universität Wien, Department of Automation, February 1999.

[351] Klaus Schossmaier and Johann Klasek. Implementing the optimal precision algorithm for clock state & rate synchronization. Technical Report 183/1-91, Technische Universität Wien, Department of Automation, February 1999.

[352] Gerald Hummel and Bettina Weiss. Random generators. Technical Report 183/1-92, Technische Universität Wien, Department of Automation, February 1999.

[353] Martin Horauer. Hardware support for clock synchronization on distributed systems. In *Proceedings of the International Conference on Dependable Systems and Networks (DSN'01)*, pages A–10–A–12, Göteborg, Sweden, July 1–4, 2001.

[354] Martin Horauer and Roland Höller. Integration of high accurate clock synchronization into Ethernet-based distributed systems. In *International Conference on Advances in Infrastructure for e-Business, e-Education, e-Science, and e-Medicine on the Internet (SSGRR'02)*, L'Aquila, Italy, January 2002.

[355] Stefan Stöckler and Gerhard-Helge Schildt. Analyse des zeitlichen Verhaltens verteilter Echtzeitsysteme. In *Proceedings Fachtagung Entwurf komplexer Automatisierungssysteme*, Braunschweig, Germany, 1992.

[356] Wolfgang Kastner, Stefan Stöckler, and Rene Zeitlberger. GOLD MINE: Specification language for event-based monitoring. In *Proceedings CONPAR'94*, pages 88–99, Linz, Austria, 1994. (Appeared in LNCS 854, Springer-Verlag).

[357] Stefan Stöckler. GOLD MINE: Generic Object-oriented Language for Defining Monitors, Events and Intervals. Technical Report 183/1-27, Vienna University of Technology, Department of Automation, April 1992.

[358] Stefan Stöckler. Timed attributed event traces. Technical Report 183/1-35, Vienna University of Technology, Department of Automation, April 1993.

[359] Stefan Stöckler. Analyzing distributed real-time systems using TATs and the specification language GOLD MINE. Technical Report 183/1-41, Vienna University of Technology, Department of Automation, May 1994.

[360] Bettina Weiss, Günther Gridling, and Markus Proske. A case study in efficient microcontroller education. In *Workshop on Embedded Systems Education (WESE'05)*, pages 36–43, September 22nd, 2005.

[361] Voin Legourski, Christian Trödhandl, and Bettina Weiss. A system for automatic testing of embedded software in undergraduate study exercises. In *Workshop on Embedded Systems Education (WESE'05)*, pages 44–51, September 22nd, 2005.

[362] Ulrich Schmid. Zukunft der technischen informatik an der tu-wien. Research Report 89/2009, Technische Universität Wien, Institut für Technische Informatik, Treitlstr. 1-3/182-1, 1040 Vienna, Austria, 2009.

Presentations

1. *Some Investigations Concerning Scheduling in Real-Time Systems*, INRIA Rocquencourt, France, 1989. **(Invited)**
2. *Monitoring in verteilten Echtzeitsystemen*, Echtzeit'91, Sindelfingen, Germany, 1991.
3. *The Average CRI-Length of a Tree Collision Resolution Algorithm in Presence of Multiplicity-Dependent Capture Effects*, ICALP'92, Vienna, 1992.
4. *The Role of Standards in Real-Time Computing*, NATO ASI on Real-Time Computing, Sint Maarten, 1992.
5. *Monitoring Distributed Real-Time Systems*, NATO ASI on Real-Time Computing, Sint Maarten, 1992.
6. *A Versatile Monitoring System for Distributed Real-Time Systems*, Safecomp'92, Zürich, 1992.
7. *On Random-Trees Arising in the Analysis of Scheduling Algorithms for Real-Time Systems*, Dagstuhl-Seminar 9328 on "Average Case Analysis of Algorithms", Germany, July 1993. **(Invited)**
8. *Synchronized UTC for Distributed Real-Time Systems*, Workshop on Real-Time Programming WRTP'94, Lake Reichenau/Germany, 1994.
9. *"Echtzeit"-Systeme* (Habilitationsvortrag), Technische Universität Wien, 1995.
10. *Interval-Based Clock Synchronization*, Dagstuhl-Seminar 9611 "Time Services", Germany, March 1996. **(Invited)**
11. *Introduction to Project SynUTC*, SynUTC-Workshop, July 1997, Technische Universität Wien.
12. *Interval-based Clock Synchronization*, SynUTC-Workshop, July 1997, Technische Universität Wien.
13. *Challenges in Interval-based Clock Synchronization*, Dagstuhl-Seminar 9728 on "Average Case Analysis of Algorithms", Germany, July 1997. **(Invited)**

14. *Internet-Based Real-Time Computing* (*Panel Discussion on Real-Time Systems*), 22nd Annual International Computer Software & Applications Conference COMPSAC'98, August 1998, Vienna, Austria. **(Invited)**
15. *Experimental Evaluation of High-Accuracy Time Distribution in a COTS-based Ethernet LAN*, 24th IFAC/IFIP Workshop on Real-Time Programming WRTP'99, Schloß Dagstuhl, Germany, May/June 1999.
16. *High-Accuracy Time Services and Fault-Tolerant Clock Synchronization*, 37th IFIP WG10.4 Annual Meeting (Workshop on "Time and Dependability"), Martinique, France, January 2000. **(Invited)**
17. *Applied Research: A Scientist's Perspective*, Keynote speech at joint 25th IFAC/IFIP Workshop on Real-Time Programming (WRTP'00) and Workshop on Algorithms and Architectures for Real-Time Control (AARTC'00), Mallorca, Spain, May 2000. **(Invited)**
18. *3 Years of START Project Y41-MAT*, Presentation for the International Jury, Austrian Science Foundation (FWF), Vienna, June 17, 2000.
19. *Embedded Systems*, Presentation at BM:vit working group meeting "IT-Strategy 2000", Oesterreichische Computer Gesellchaft OCG, August 3, 2000.
20. *How to model link failures: A perception-based fault model*, International Conference on Dependable Systems and Networks (DSN'01), Göteborg, Sweden, July 1–4, 2001.
21. *Ein "Versuch über die wahre Art, das Clavier zu spielen"*, Berufungsvortrag Embedded Computing Systems, TU Wien, Vienna (Austria), December 18, 2001.
22. *Formally verified byzantine agreement in presence of link faults*, 22nd International Conference on Distributed Computer Systems (ICDCS'02), July 2002, Vienna, Austria.
23. *Forschungsschwerpunkt Technische Informatik*, Kick-Off-Event Informatik-Netzwerk IN:N der TU-Wien, Vienna, Austria, 30. September 2002.
24. *Hybrid Process and Link Failures in Synchronous, Partially Synchronous and Asynchronous System Models*, Faculty of Computer Science, University of Lisboa, 28. Jänner 2003
25. *Randomized Asynchronous Consensus with Imperfect Communications*, 22nd Symposium on Reliable Distributed Systems (SRDS'03), Florence, Italy, October 6–8, 2003
26. *2004 Research Topics*, Embedded Computing Systems Group E182/2, TU-Wien, 17. Oktober 2003
27. *Embedded Systems an der TU-Wien*, FIT-IT Workshop 2003, Siemens, Wien, 17. Jänner 2003
28. *Asynchronous Distributed Real-Time Systems? An Overview of Future ECS Research*, Institut für Technischen Informatik, TU-Wien, 20. März 2003
29. *Institut für Technische Informatik: Embedded Computing Systems Group*, Institut für Technischen Informatik, TU-Wien, 29. September 2003
30. *The* Θ*-Model*, INRIA Rocquencourt, Versailles, 3. September 2004
31. *The* Θ*-Model*, 2. ASSERT RC/SF-Meeting, TU-Vienna, 20. September 2004
32. *The* Θ*-Model*, Diskussionskreis Fehlertoleranz (DFT'04), Humboldt-Universität Berlin, 12. November 2004
33. *IKT in Österreich 2006: Wissenschaftliche Forschung - Quo vadis?*, BM:vit Tagung IKT Forschung Österreich: Herausforderung, Chancen und Positionierung, Wien, Palais Strudlhof, 5.–6. Dezember 2006. **(Invited)**
34. *Keynote: A Perspective of Fault-Tolerant Clock Synchronization*, International IEEE Symposium on Precision Clock Synchronization for Measurement, Control and Communication (ISPCS'07), October 1-3, 2007, Austrian Academy of Sciences, Vienna, Austria. **(Invited Keynote)**
35. *Distributed Algorithms and VLSI — An Appetizer*, Dagstuhl-Seminar 08371 on "Distributed Algorithms on VLSI Chips" (Organizers: Bernadette Charron-Bost, Jo Ebergen, Shlomi Dolev, Ulrich Schmid), SchloßDagstuhl, Germany, September 7–10, 2008.
36. *Challenges in Fault-Tolerant Distributed Real-Time Systems*, RiSE Workshop, TU Graz, January 22, 2010.
37. *Reconciling Distributed and Real-Time Computing*, RiSE Hearing, Austrian Science Foundation (FWF), Vienna, July 2, 2010.
38. *Invited Tutorial: Synchrony and Time in Fault-tolerant Distributed Algorithms*, Formal Modeling and Analysis of Times Systems Conference (FORMATS'10), IST Austria, September 8–10, 2010. **(Invited Tutorial)**
39. *Distributed Algorithms*, Joint VCLA/RiSE Winter School on Verification, February 6-10, 2012, Vienna.
40. *Technische Informatik an der TU Wien*, HTL St. Pölten, May 2012.
41. *Technische Informatik Universittsstudium und HTL Ausbildung: Chancen und Herausforderungen*, Fachwissenschaftliches Koordinationsseminar der Pädagogischen Hochschule für NÖ, HTBLuVA Salzburg, December 2012.
42. *Fault-Tolerant Distributed Algorithms*, RiSE Winter School on Verification, February 11-15, 2013, Vienna.

43. *Parameterized Verification Challenges in Distributed Algorithm*, RiSE Workshop, November 19, 2013, Vienna.

44. *Easy Impossibility Proofs for k-Set Agreement*, Dagstuhl-Seminar 16282 on *Topological Methods in Distributed Computing*, July 10–15, 2016, Schloss Dagstuhl–Leibniz-Zentrum fuer Informatik.

45. *Reconciling Fault-Tolerance and Robustness ?*, Workshop on Design and Analysis of Robust Systems @ CPS-Week 2016, Hofburg, Vienna, Austria, April 11, 2016. **(Invited talk)**