

Curriculum Vitae

ULRICH SCHMID

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Personal data:

Surname Schmid
First name Ulrich
Title Univ.Prof. Dr.techn. Dipl.Ing.
Email, Homepage s@ecs.tuwien.ac.at, <http://ti.tuwien.ac.at/ecs/people/schmid>
Birth February 22, 1960 in Randegg (Lower Austria)
Citizenship Austrian
Religion Roman catholic
Family status Married to Dr. Isolde Schmid-Reiter, Ass. Prof. at University of Vienna & Secretary General of European Academy of Music Theatre
Private interests Music (organist), philosophy, literature, athletics

Education:

1974–1979 Höhere Technische Lehranstalt St. Pölten (Communications Technology and Electronics)
1979 Matura (with distinction)
1979–1980 Army service
1981–1986 Studies at TU-Wien (Computer Science, Mathematics)
1985 Diploma Computer Science (with distinction)
1986 Dr. techn. (with distinction)

Professional activities:

1980–1981 Industrial electronics with company Ing. Steiner, Vienna
1982–1987 Own business (embedded systems)
1987–1988 Research Assistant at
Department of Algebra und Discrete Mathematics, TU-Wien
1988–1995 Assistant professor at
Department of Automation, TU-Wien
1995 Habilitation for the entire field of “Informatik”
1995–2003 Associate professor at TU-Wien, Department of Automation
2003–now Full professor for Embedded Computing Systems, TU-Wien
2010 Teaching at Institute of Science and Technology, Austria

Own Publications

Year Journal papers

2016 [1, 2]
2015 [3, 4]
2014 [5, 6, 7, 8]
2013 [9, 10]
2012 [11, 12]
2011 [13, 14]
2010 [15]
2009 [16, 17, 18]
2008
2007 [19]
2006 [20]
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2004 [21]
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2002
2001 [22]
2000
1999 [23, 24]
1998
1997 [25, 26, 27]
1996 [28]
1995 [29]
1994 [30, 31, 32, 33, 34, 35]
1993
1992 [36]
1991 [37, 38]
1990 [39, 40]
1989 [41, 42, 43]
1988 [44]
1987 [45]
1983 [46]

Year Books

2009
1996
1990 [131]

Year Conference papers

2016 [47, 48, 49]
2015 [50, 51, 52]
2014 [53, 54, 55]
2013 [56, 57, 58, 59, 60, 61, 62, 63, 64]
2012 [65, 66]
2011 [67, 68, 69, 70, 71]
2010 [72, 73, 74, 75, 76]
2009 [77, 78, 79, 80]
2008 [81, 82, 83, 84, 85]
2007 [86, 87]
2006 [88, 89, 90, 91, 92, 93]
2005 [94, 95, 96, 97]
2004 [98]
2003
2002 [99, 100, 101]
2001 [102, 103]
2000 [104, 105, 106, 107, 108]
1999 [109, 110]
1998 [111, 112, 113, 114]
1997 [115]
1996 [116, 117, 118]
1995 [119]
1994 [120, 121]
1993 [122, 123, 124]
1992 [125, 126, 127, 128]
1991 [129, 130]
1990
1989
1988
1987
1983

Editorials

2009 [132]
1996 [133]
1990

Year	Technical Reports	Year	Other publications
2016	[134, 135, 136, 137]	2016	[223]
2015	[138, 139]	2015	[224]
2014	[140, 141, 142, 143]	2014	[225]
2013	[144, 145]	2013	[226]
2012	[146, 147, 148]	2012	[227, 228, 229, 230, 231, 232]
2011		2011	
2010	[149, 150]	2010	
2009	[151, 152, 153]	2009	
2008	[154, 155]	2008	
2007	[156, 157, 158, 159]	2007	
2006	[160, 161, 162, 163, 164]	2006	[233]
2005		2005	[234]
2004	[165, 166, 167, 168, 169, 170, 171, 172]	2004	
2003	[173, 174, 175, 176, 177, 178]	2003	
2002	[179, 180]	2002	[235]
2001	[181, 182, 183, 184, 185, 186, 187]	2001	[236]
2000	[188, 189, 190, 191, 192]	2000	
1999	[193, 194, 195, 196, 197, 198]	1999	
1998	[199, 200, 201, 202]	1998	
1997	[203, 204]	1997	[237, 238]
1996	[205, 206, 207]	1996	[239]
1995	[208, 209, 210]	1995	
1994	[211]	1994	[240]
1993	[212, 213, 214, 215]	1993	[241]
1992	[216, 217]	1992	
1991	[218, 219, 220, 221, 222]	1991	
1986		1986	[242]
1985		1985	[243]

Statistics

Art	#	#best	#invit.	$\sum p.$	Avg.p.	Min.p.	Max.p.
Journals	46		6	1039	23	3	75
Conferences	82	4	6	720	9	1	26
Books	1			400	400	400	400
Editorials	2			420	210	60	360
Technical Reports	89			3445	39	3	400
Others	21			352	17	1	132
Sum:	241	4	12	6376			

Supervision

Year	Dissertations	Year	Masters/Diplomas
2014	[244]	2014	
2013		2013	[259, 260, 261, 262]
2012		2012	[263]
2011	[245]	2011	
2010	[246]	2010	[264, 265]
2009	[247, 248]	2009	
2008		2008	
2007		2007	
2006	[249]	2006	[266]
2005	[250, 251]	2005	[267]
2004	[252, 253]	2004	[268]
2003		2003	
2002	[254]	2002	[269, 270, 271]
2001		2001	
2000		2000	[272, 273]
1999	[255]	1999	[274]
1998	[256]	1998	
1997		1997	[275, 276]
1996	[257]	1996	[277, 278]
1995		1995	[279]
1994	[258]	1994	[280, 281, 282, 283]
1993		1993	
1992		1992	[284]
1991		1991	[285]

Some Highlights . . .

Research

- (Co-)Author of 130+ journal and conference publications; supervisor of 100++ publications of group members
- Austrian START price (1996), Kardinal Innitzer Förderungspreis (1995)
- Several best papers [83, 66], invited papers [14, 23] and keynotes [81, 286]
- Several patents [167, 189]
- Selected accomplishments:
 - Models for fault-tolerant distributed algorithms in VLSI circuits [1, 50, 6, 10, 11]
 - Agreement in distributed systems with process and link failures [47, 287, 65, 16, 13, 99]
 - Partially synchronous system models [17, 94, 18, 287, 14]
 - Interval-based clock synchronization [24, 29, 23]
 - Distributed computing models for real-time systems [7, 85]
 - Automatic competitive analysis of real-time systems [55, 57]
 - Analytic combinatorics in queueing systems analysis [38, 33]
- PC-member in many scientific conferences (PODC, DISC, OPODIS, ICDCS, IPDPS, EDCC, SSS, etc.)
- Associate editor J. Real-Time Systems (until 2010), J. Scheduling (until 2004)

Teaching

- Supervisor of 10+ PhD and 25+ Master theses
- Rich experience in design and teaching of courses in the areas fault-tolerant distributed algorithms and real-time systems
- Co-author of textbook *Informatik* (Springer, 3 editions) [131]

Management and Administration

- Acquisition of 15+ big research projects, including

<i>Leader</i>	<i>Title</i>	<i>Funding</i>	<i>Agency</i>	<i>Duration</i>
U. Schmid	Fault-Tolerant Asynchronous Logic (FATAL)	EUR 451k	FWF/ P21694	2009–2014
U. Schmid	NFN Rigorous Systems Engineering (RiSE+SHiNE) PP05: Reconciling Distributed and Real-Time Computing	EUR 749k	FWF/ S11405	2011–now
U. Schmid	Gracefully Degrading Agreement in Directed Dynamic Networks (ADynNet)	EUR 350k	FWF/ P28182	2016–now

- Designer and coordinator of Bachelor and Master curriculum “Technische Informatik”
- Coordinator of major research focus “Technische Informatik” at TU-Wien
- Many faculty administration and planning duties (quality management, capacity planning, etc.)

Detailed Information . . .

Research

Brief description of the primary goals in scientific research:

- Knowledge-driven scientific investigation of relevant and difficult problems in all areas of computer engineering.
- Quality before quantity.
- Creation of an optimal research climate based upon freedom and achievement motivation.
- Primary focus on leading own (TU Wien) students towards internationally competitive research.
- Setup of cooperations with competent—and, if possible, locally available—experts in all project-relevant disciplines.
- Demonstration of relevance of the pursued research by stimulating the transformation of scientific results into prototype implementations/industrial pilot applications.

Prices, Awards and Invitations

- START price of the Ministry of Science and Research (1996, see [205, 237, 188, 236]), the most prestigious award for young scientists in Austria; EUR 1.000.000,— freely available research funding for 6 years.
- Kardinal Innitzer-Förderungspreis (1995) for the accomplishments of the “Habilitationsschrift” [33].
- Best papers: IFAC WRTP’94 [124], WRTP’99 [112], SSS’08 [83], DSD’12 [66].
- Invited keynotes and tutorials: IFAC WRTP’2000 [105], ISPCS’07 [286], SSS’08 [81], FORMATS’10 [75], DARS’16 [288]
- Invited panels and seminars: Panel COMPSAC’98 [113], several Dagstuhl seminars [241, 239, 238, 289, 223]
- Invited Papers: Control Engineering Practice [22, 30], J. Real-Time Systems [23], e&i [21, 20], Theoretical Computer Science [14], Microprocessors and Microsystems [10].

Supervised PhD Theses

1. Alexander Kößler. Real-Time Performance Analysis of Synchronous Distributed Systems. 2014.
2. Peter Robinson. Weak System Models for Fault-Tolerant Distributed Agreement Problems. 2009.
3. Matthias Függer. Analysis of On-Chip Fault-Tolerant Distributed Algorithms. 2010.
4. Martin Biely. Dynamic Aspects of Modeling Distributed Computations. 2009.
5. Heinrich Moser. A Model for Distributed Computing in Real-Time Systems. 2009 (summa cum laude; Promotion “sub auspiciis praesidentis”).
6. Hannes Stratil. Advantages and Limitations of Position-based Communication in Wireless Ad-hoc Networks. 2006.
7. Martin Hutle. Failure Detection in Sparse Networks. 2005.
8. Bernd Thallner. Topology Control for Fault-Tolerant Communication in Wireless Ad Hoc Networks. 2005.
9. Josef Widder. Distributed Computing in the Presence of Bounded Asynchrony. 2004.
10. Bettina Weiss. Authenticated Consensus. 2002.
11. Klaus Schossmaier. Interval-based Clock State and Rate Synchronization. 1998.
12. Dietmar Loy. GPS-Linked High Accuracy NTP Time Processor for Distributed Fault-Tolerant Real-Time Systems. 1996.
13. Stefan Stöckler. Event-based monitoring of distributed real-time systems. 1994.

PhD co-supervisor:

1. Samar Khattab. Efficient Interference Reduction in Low Complex Digital Direct Sequence Spread Spectrum Systems. Faculty of Electrical Engineering and Information Technology, TU-Vienna, 2010.

External PhD thesis committee member:

1. Andreas Pavlogiannis (IST Austria)
2. Thomas Nowak (Ecole Polytechnique Paris)

Activities in the Scientific Community

- General chair DISC'17, October 2017, Vienna (with J. Widder)
- Organizer Dagstuhl-Seminar 08371 “Fault-Tolerant Distributed Algorithms in VLSI Chips” (with Jo Ebergen, Bernadette Charron-Bost und Shlomi Dolev) [289], Dagstuhl castle, Germany, September 2008.
- Associate Editor for Journal of Scheduling (until 2004), J. Real-Time Systems (until 2010).
- Program committee member of WRTP'00, DSN'01, DISC'01, WRTP'03, SenSys'04, WRTP'04, OPODIS'05, DIWANS'06, OPODIS'06, PODC'07, SSS'08, IPDPS'09, EDCC'10, ICDCS'10, WRAS'10, IPDPS'10, ICDCS'11, ICDCS'11, LAFT'11, EDCC'11, SSS'12, ICDCN'12, EDCC'12, SIROCCO'13, EDCC'14, SOFSEM'15, DISC'15, ICDCN'16, CERTS'16
- Research management policies:
- Member in steering committee of the BM:vit research funding (programme FIT-IT “Embedded Systems”, until 2012).
- Project reviews for National Science Foundation, IRISA, Israel Science Foundation.
- Tenure reviews for TU-Wien, UCSD, EPFL, Ecole Polytechnique Paris, INRIA, Technion Haifa.
- Paper reviews for international journals and conferences: Algorithmica, ICALP, Information and Computation, ISADS, J. Algorithms, Real-Time Systems, Software Practice & Experience, The Computer Journal, Theoretical Computer Science, IEEE Transactions on Parallel and Distributed Systems, IEEE Transactions on Networks, J. Scheduling, J. Systems Architectures, IEEE Transactions on Computers, ACM Computing Surveys, IEEE Transactions on Software Engineering, Distributed Computing, SIAM J. Computing, Journal of Applied Logic, J. of Circuits, Systems, and Computers, J. Software Testing and Verification; WRTP, DISC, DSN, CCN, PODC, IFAC World Congress, OPODIS, SenSys, DIWANS, SSS, IPDPS, EDCC, ICDCS, SIROCCO, WRAS, LAFT, ICDCN, STOC, SOFSEM, CERTS.

Memberships

Overview Research Projects

- Project **Rigorous Systems Engineering** (RiSE+SHiNE, <http://arise.or.at>), see [57, 58, 59, 63, 64, 55, 225, 3, 288, 223] and [290, 291, 244]. Supported by Austrian Science Fund (FWF) National Research Network (NFN) S11405 [Project part PP05: Reconciling Distributed and Real-Time Computing], in collaboration with H. Veith (TU Wien), K. Chatterjee (IST Austria) and E. Bartocci (TU Wien, sub-task leader PP05 SHiNE).

Devoted to the application of formal verification methods to problems in distributed computing and real-time computing. Core results are a method for parameterized model checking of fault-tolerant distributed algorithms [63] and applying algorithmic game theory for competitive analysis of real-time scheduling algorithms [57, 55].

- Project **Fault-tolerant Asynchronous Digital Circuits**, see [154, 152, 77, 72, 67, 11, 66, 12, 227, 228, 229, 230, 231, 232, 9, 10, 56, 60, 61, 62, 226, 53, 5, 6, 140, 50, 51, 4, 224, 1, 2] and [292, 246, 293, 263, 261, 262]. Supported by the Austrian Science Fund (FWF) project P21694 [Fault-tolerant Asynchronous Logic (FATAL) <http://ti.tuwien.ac.at/ecs/research/projects/fatal>], a collaboration with the Institute of Electrodynamics, Microwave and Circuit Engineering and the Institute of Atomic and Subatomic Physics at TU-Wien. International collaborations with D. Dolev (Hebrew University Jerusalem) and C. Lenzen (MPI Saarbrücken), Kay-Obbe Voss (GSI Darmstadt) and Ulrich Giesen (PTB Braunschweig), and by the FWF projekt P26436 [Self-stabilizing Byzantine Fault-Tolerant Distributed Algorithms for Integrated Circuits (SIC) <http://ti.tuwien.ac.at/ecs/research/projects/sic>].

Development of the mathematical/formal foundations of a framework for the hierarchical modeling and analysis of fault-tolerant asynchronous VLSI circuits, using fault-tolerant distributed algorithms knowledge in conjunction with the experimental assessment of both radiation-induced failures and metastability in modern VLSI technology. Core results are a suitable computing and system model [11], including an extension to self-stabilizing algorithms [6], digital [10] and analog [12] modeling of single-event transients, and digital modeling of glitch-propagation and metastability [1, 51]. Applications: Self-stabilizing Byzantine fault-tolerant clock generation [5, 6] and clock distribution [2] in SoCs.

Publications appeared in first-rate journals und conference proceedings; best paper award [66], invited paper [10].

- Project **Partially synchronous models for distributed systems**, see [175, 173, 174, 178, 165, 98, 94, 95, 97, 91, 161, 92, 17, 18, 82, 83, 14, 85, 155, 80, 153, 79, 68, 69, 145, 7, 8] and [294, 295, 296, 297, 251, 298, 299, 300, 301, 247, 248, 245]. Supported by the FWF projects P17757 [Asynchronous Distributed

Algorithms in the Θ -Model (Theta), <http://ti.tuwien.ac.at/ecs/research/projects/theta>], P20529 [Partially Synchronous Distributed Real-Time Systems (PSRTS), <http://ti.tuwien.ac.at/ecs/research/projects/psrts>)] and the FIT-IT “Embedded Systems” PhD stipend 808198 [Distributed Computing in the Presence of Bounded Asynchrony (DCBA)]. International collaborations e.g. with G. LeLann (INRIA Rocquencourt), Ch. Fetzer (TU Dresden) and D. Malkhi (Microsoft Research).

Definition and investigation of novel partially synchronous system model, which allows the definition of asynchronous algorithms for fault-tolerant distributed real-time systems. Core results are the Θ -Model [97], the FAR model [94], the WTL model [18, 80] and the ABC model [14]; focus on k -set agreement [80, 69]. Real-time scheduling analysis is supported by the real-time distributed computing model [91, 299]. Promising applicability in the area of VLSI Systems-on-Chip [11, 72].

Publications appeared in first-rate journals and conference proceedings; best Paper Award [83], invited paper [14], keynote [81] and tutorial [75].

- Project **Distributed Algorithms for Robust Tick-Synchronization** (DARTS, <http://ti.tuwien.ac.at/ecs/research/projects/darts>), see [168, 167, 89, 93, 88, 160, 162, 159, 86, 20, 84, 81, 132, 78, 77, 72, 11] and [302, 266, 303, 292, 246, 264, 304]. Joint project with Austrian Aerospace (now Ruag Austrian Aerospace). Supported by the award-winning FIT-IT “Embedded Systems” project 809456 (DARTS).

Application of asynchronous fault-tolerant Θ -algorithms in VLSI systems-on-chip. Central results are mathematical correctness proofs and performance analyses [11, 72] as well as a complete ASIC implementation [304].

International patent application [167] and invited paper [20]. Organization of a Dagstuhl seminar [132] and invited keynote [81] at SSS’08.

- Project **Fault-tolerant Distributed Algorithms in Dynamic Networks**, see [31, 210, 196, 188, 107, 192, 186, 102, 182, 181, 103, 187, 180, 179, 99, 305, 177, 172, 171, 170, 166, 169, 306, 307, 90, 19, 15, 18, 16, 308, 74, 73, 70, 65, 54, 52, 47, 223, 48] and [309, 310, 311, 312, 313, 314, 315, 316, 254, 269, 270, 317, 318, 319, 320, 321, 322, 323, 324, 325, 326, 327, 328, 329, 330, 331, 326, 267, 250, 251, 249, 332, 333, 233, 334, 335, 300, 248, 259, 260]. Supported by the Austrian START price Y41-MAT [project W2F <http://www.ecs.tuwien.ac.at/projects/W2F/>] and the FWF projekts P18264 [Fault-Tolerant Distributed Algorithms in Sparse Ad Hoc Wireless Networks (SPAWN), <http://ti.tuwien.ac.at/ecs/research/projects/spawn>] and P28182 [Gracefully Degrading Agreement in Directed Dynamic Networks (ADynNet) <http://ti.tuwien.ac.at/ecs/research/projects/adyndnet>]. International collaborations with I. Keidar (Technion Haifa), D. Malkhi (Microsoft Research), A. Schiper (EPFL), B. Charron-Bost (Ecole Polytechnique Paris), T. Nowak (ENS Paris), M. Biely (EPFF) and P. Robinson (NSU Singapur).

Development of the theoretical and algorithmic foundations for fault-tolerant distributed real-time systems based on incomplete and/or highly time-varying communication topologies, e.g., wireless ad-hoc networks. Major achievements comprise a hybrid failure model for process and link failures, fault-tolerant communication and Voronoi-aided routing, algorithms for system booting, and failure detectors for sparse communication graphs. Systematic exploration of agreement (consensus, k -set agreement etc.) in directed dynamic networks [65, 52, 47].

- Project **Synchronized Universal Time Coordinated for Distributed Real-Time Systems** (SynUTC, <http://www.ecs.tuwien.ac.at/SynUTC/>), see [30, 29, 28, 25, 26, 23, 24, 124, 118, 115, 111, 112, 109, 110, 104, 106, 192, 212, 211, 208, 239, 207, 203, 204, 238, 27, 200, 114, 193, 194, 195, 197, 188, 189, 183, 100, 101], [133, 286] and [283, 279, 336, 337, 257, 277, 338, 339, 340, 275, 276, 341, 342, 343, 344, 256, 345, 274, 346, 347, 348, 349, 350, 252]. Supported by the Austrian Science Fund under grant P10244-ÖMA, the Austrian START-Programme Y41-MAT, the Austrian Ministry of Science under contract ZI.601.577/2-IV/B/9/96, and the Austrian National Bank (OeNB) under grant 6454. Joint project with the Department of Computer Technology (TU-Wien) and the Department of General Electrical Engineering and Electronics (TU-Wien).

Development of theoretical foundations and hardware+software for providing a highly accurate global time in distributed fault-tolerant real-time systems. Interval-based approach, utilizing an integration of clock synchronization and GPS satellite receivers. Major achievements e.g. an elaborate hardware support (UTCSU-ASIC), novel clock synchronization algorithms, a powerful simulation framework, and a comprehensive mathematical/formal and experimental analysis. Best papers at IFAC WRTF’94 [124] und WRTF’99 [112], best student paper DSN’01 [349]; solution to the more than 10-year-old problem of finding a fault-tolerant intersection function satisfying a Lipschitz condition (L. Lamport) [24].

Papers published in first-rate international journals and conference proceedings. Many invited papers and talks [30, 23, 109, 104, 105, 239, 238]; presentation at the “Hannover Messe’98” [200]; Patents [204, 189] and industrial pilot applications. Further exploitation of results by spin-off company *Oregano Systems* in the context of FIT-IT projec PSynUTC. Keynote speech at ISPCS’07 [286].

- Project **Versatile Timing Analyzer** (VTA) for monitoring of distributed real-time systems, see [36, 129, 125, 126, 127, 123, 120, 221, 216, 213] and [351, 352, 353, 354, 355]. Supported by the Austrian Science Fund under grant P8390-TEC.

Foundations and Development of a general-purpose monitoring systems for timing analysis in distributed real-time systems. Major achievements e.g. maximum target-system independent, runtime code-instrumentation, object oriented event definition language with formal semantics, and distributed event recognition and processing.

- Project **Performance Models and Load Assumptions for Scheduling in Soft Real-Time Systems** (topic of Habilitationsschrift), see [42, 43, 39, 40, 37, 32, 33, 241, 218, 206].

Mathematical/theoretical quantification of *deadline meeting capabilities* of scheduling algorithms for probabilistic aperiodic tasks in real-time systems. Utilization of advanced combinatorial and asymptotic methods allows a respective performance analysis without stable state assumptions.

Papers—including Habilitationsschrift—published in first-rate international journals; presentation at Dagstuhl-Seminar “Average Case Analysis of Algorithms”.

- Project **Broadcast Random-Access Communications in Computer Networks, Models and Analysis** (Department of Algebra und Discrete Mathematics), see [45, 44, 41, 38, 130, 242, 219, 217]. Supported by the Austrian Science Fund (FWF) under grant P6477P.

Mathematical/theoretical investigation of characteristic parameters (primarily throughput and stability) of protocols for multiple access broadcast networks à la Ethernet. Results are e.g. the solution of the 20-year-old problem of the *time-to-instability* of ALOHA networks and a thorough investigation of the impact of *channel capture*.

Development activities

Development Activities in Research Projects

Software and hardware development of systems supporting research projects or transforming research results into prototype systems:

- General outline of the *Primitive Event Management* (target interface, external event recognition) of our *Versatile Timing Analyzer* VTA.
- Object-oriented design of the VTA software (CRC-Cards) and basic considerations concerning the human interface, in particular data analysis and visualization.
- Design of our *Distributed Object-Based Operating Systems* DOBOS built on top of SunOS and pSOS^{+m} to be used for the VTA, see [119, 116, 214].
- Hardware architecture of a 802.3DCR LAN coprocessor for a Force M68030 VMEbus CPU-30 (for projects VTA und SynUTC).
- Planning of measuring equipment for experimental long-term evaluation of GPS satellite receivers (for project SynUTC), see [115].
- Specification and architecture of the Network Time Interface (NTI) M-Module (for Project SynUTC), see [207, 194].
- Concept of a high-performance device driver for the abovementioned LAN coprocessor, for integration in a pSOS^{+m} multiprocessor system.
- Low-level programming of the NTI and HW/SW debugging of AcQ i6360 and MEN A203 M-Module carrier boards, see [193].
- Redesign, test and evaluation of the NTI Device-Driver + NTI on Motorola’s MVME-162 CPU under pSOS^{+m}, see [195].
- Specification and setup GPS Device-Driver for the NTI, see [197].
- Setup of a pSOS^{+m} development environment for MVME-162 CPUs.
- Development of an embedded clocksynchronization demo application for SynUTC, see [110].
- Installation und Setup Lauterbach-Debugger for PowerPC MPC555- and M68040-Targets under Enea OSE.
- Collaborative work on specification of professional implementation of SynUTC software and hardware (FIT-IT project PSynUTC by spin-off company Oregano Systems) [183].
- Development of a SynUTC-synchronized networked embedded system using MPC555 und MPC860 CPUs under OSE [273].
- Definition, coordination and participation in building up HW and SW of FIDIS cluster (20 Ethernet+CAN-coupled MEN EM1N PowerPC microcontrollers, QNX Neutrino RTOS, Lauterbach development tools)

Development Projects with own Business (1982–1991)

Development projects in the area of microprocessor systems and industrial electronics:

- Development of a second generation *Informator*-system (for Tirolean tourist agency).
- Development of a multitasking operating system kernel (SMX-65) for 6502 microprocessors.
- Development of a high-level macro language for assembler programming, see [46].
- Development and production of a programmable controlling system for oil-fueled heating installations.
- Development and production of a teaching aid for courses on aural training for students in music (Musikakademie Graz).
- Development of a multiuser telex system for office automation (sold by company Ph. Liebisch, Vienna).

Industrial Employment with Company Ing. Steiner, Vienna (1980–1981)

Work on development projects in the area of microprocessor systems and industrial electronics:

- In-circuit emulator for microprocessor 6502.
- Bus-coupler *Commodore Bus* to Steiner “Puzzle”-Bus.
- Miscellaneous (production-)test software, e.g. for parallel I/O board and floppy controller.
- Data acquisition system for automated book printing (for the Austrian publisher *Überreuter*).
- Remote accommodation service system *Informator* (pilot project for the tourist office Kitzbühel).

Patents

Patents (applied personally or via firms) on results of own research.

1. Baur Prüf- und Meßtechnik (A-6832 Sulz, Austria): *Energiekabel-Fehlerortung*, see [204]
2. Nikolaus Kerö, Ulrich Schmid, Martin Horauer: *Uhrensynchronisation in Netzwerken*, see [189]
3. Ulrich Schmid, Andreas Steininger: *Dezentrale Fehlertolerante Taktgenerierung in VLSI Chips*, see [167]

Teaching

Own courses

Verteilte Algorithmen (2004-now)

6 ECTS mandatory lecture + practical in Master curriculum “Technische Informatik”, based on the book *Distributed Algorithms* by H. Attiya und J. Welch.

Seminars

- 3 ECTS mandatory seminar **Scientific Working** in Bachelor curriculum “Technische Informatik” (2011–now). Introduction to scientific working and scientific communities; literature search; writing, reviewing and presentation of a scientific paper.
- 3 ECTS mandatory seminar **PhD Primary Area Computer Engineering Introduction** for Vienna PhD School of Informatics (2009–2013, jointly with A. Steininger).
- 3 ECTS optional research seminar **Rigorous Systems Engineering** (jointly with Helmut Veith und Tom Henzinger/IST Austria)
- 3 ECTS Pflichtproseminar **Wissenschaftliches Arbeiten** (1992–2006).

Real-Time Scheduling (2005-now)

3 ECTS optional lecture + practical in Master curriculum “Technische Informatik”, based upon the book *Deadline Scheduling for Real-Time Systems* by J. Stankovic, M. Spuri, K. Ramamritham and G. Buttazzo.

Building Reliable Distributed Systems (2011-now)

4.5 ECTS optional practical in Master curriculum “Technische Informatik” (jointly with M. Függer and A. Kößler). Implementation of simple distributed algorithms on microcontroller boards running a real-time operating system (QNX, VxWorks, RTLinux).

Problems in Distributed Computing (2011-now)

3 ECTS optional lecture + practical in Master curriculum “Technische Informatik”. Introduction of advanced topics in distributed algorithms; joint reading and student’s presentations of selected scientific papers.

Supervision

Supervision of practical [35] and scientific projects, Bachelor theses, Master/Diploma theses and dissertations.

Advanced Distributed Algorithms (IST Austria, 2009)

Three hours lecture + practical am Institute of Science and Technology (IST) Austria, for PhD Students der PhD School of Informatics an der TU-Wien und der PhD School am IST Austria.

Distributed Algorithms for Fault-Tolerant Real-Time Systems (2007-2010)

Two hours optional lecture + practical devoted to real-time scheduling in networked distributed systems.

Ausgewählte Kapitel der Technischen Informatik X (1998–2006)

Two two-hours lecture + practical devoted to distributed algorithms for introducing interested students to our research projects. Individual work + presentation of the solution of a scientific problem.

Lecture + Practical “Modellierung, Design und Analyse von Echtzeitsystemen” (1992–2002)

2+2-hour special course (lecture+practical) for students of *Technical Computer Science*, devoted to an introduction into the industrial state-of-the-art in embedded systems’ design. Utilizes hardware/software environment of the practical “Prozeßautomatisierung”.

Practical “Prozeßautomatisierung” (1989–1992)

Basic course in computerized automation for all students of computer science.

- **1989–1992:** Definition of content, implementation and running the course for about 300 participants/year, see [220], [122].
- **1993–2000:** Design of a new course devoted to embedded systems in computerized automation. Major responsibility for contents, implementation and running the practical for about 200 participants/year, see [121, 117, 34, 190].
- **2000–2002:** Design of a new 1,5 hours/week process-control-oriented basic course on computerized automation. Major responsibility for concept, contents and organization of the practical for about 200 participants/year.

Lecture “Einführung in die Informatik I” (1989–1992)

Introductory course in computer science (Prof. G.-H. Schildt). “Architect” and co-author of the text-book *Informatik*, see [131].

Other Activities Related to Teaching

FIT-IT Projekt Seamless Campus - Distance Labs (SC-DL)

BM:VIT FIT-IT Embedded Systems accompanying measures project (SC-DL, <http://ti.tuwien.ac.at/ecs/research/projects/scdl>), devoted to the development of a distance learning concept for the labs Microcontroller (carry-out equipment) and Digital Design (remote workplaces), including a web portal for the whole “Technische Informatik” at TU-Wien [356, 357].

Miscellaneous

- Course evaluations and quality assessment
- Presentation Bachelor curriculum “Technische Informatik” (Beginner’s Day, Info Day, etc.)
- Student selection and comprehensive exam in primary area “Computer Engineering” in PhD School of Informatics of TU Wien (until 2012)

Administration

Activities at the Institut für Technische Informatik/Embedded Computing Systems Group (2003–now)

- Founded by appointing me professor and head of the former VLSI-Design Group in 2003:
 - Development and dissemination of mission, goals and strategy of the new ECS group
 - Identifying joint research work
 - Planning of renovation and new furniture
 - Supervision of planning a chipcard-based access control and video surveillance system of ECS group + Informatik-Labor Treitlstraße
 - Financing scheme and budgets negotiation
- Global activities related to the institute
 - Development of institute’s organization guidelines
 - Planning and supervision/coordination of maintenance and extension of the TI Web-Portal
 - Content provision for TI Web-Portal
- Integration of Computer Architecture professor (M. Shafique)

Activities at the Department of Automation (1988-2003)

- Building up the department’s infrastructure (when Prof. G.-H. Schildt was appointed to the departments head in 1988):
 - Planning and purchase of the workstation network and other equipment: HP/Apollo-Workstations, peripherals, software
 - UNIX system management, see [222]
- Management of Department’s funds, including planning and purchase of new equipment
- Planning of extension/rebuilding of the department
- Writing the department’s activity reports

Membership in faculty committees

- Gerätekommission der Fachgruppe Informatik (1988–now)
- Institutskonferenz (1988–1991)
- Fakultätskollegium (1990–1994)
- Kommission zur Vergabe von Leistungs- und Förderungsstipendien der Fakultät (1992–1999)
- Budget- und Stellenplankommission der Fakultät (1995–1999)
- Raumplanungskommission der Fakultät (1995–1999, 2007)
- Fakultätsrat (2004–now)
- Studienkommission Informatik (2004–now)
- Advisory-Board of the Dean (2011–now)
- Jury Epilog (Master thesis award), Siemens PhD-Stipend
- Berufungskommission “Interaktive Systeme”, “Embedded Systems” (Faculty of Electrical Engineering), “Algorithmen und Datenstrukturen”, “Security”, “Computer-Aided Verification”, “Parallel Computing”, “Dependable Systems”, “Systems-on-Chip” (Fakultät Elektrotechnik), “Security”, “Ubiquitous Computing”, “Computer Architecture”
- Candidate reviews for professorship “Diskrete Mathematik” (Fakultät Mathematik)
- Habilitationskommissionen
- Directing committee member PhD-School of Informatics (until 2012)
- Speaker of the faculties Professorenkurie (2016–now)

Structural Concepts for Faculty and TU-Wien

- Development of model for capacity planning and staff disposition for faculty, see [199]
- Development of model for capacity planning and staff disposition for Fachgruppe Informatik, see [199, 201]
- Assessment of teaching load vs. capacity for faculty [198]
- Development of a computer lab organization plan for the faculty, see [202, 184]
- Participation in the definition of the development plans of the faculty [358]
- Coordinator of the major research focus “Technische Informatik”
- Designer and coordinator of the Bakkalaureats- and Magisterstudium “Technische Informatik” (2002–now) [185]
 - Head of working group
 - Initial proposals
 - Coordination with faculty of electrical engineering, mathematics and physics.
 - Coordination with IST Austria
- Development of a course admission control strategy (“Score-Model”)
- Development and coordination of a *Bachelor with Honors* program

Creation of Laboratories and Infrastructure

- Building up the Informatik-Labor Treitlstraße 1 (1993–1994), primarily dedicated to the courses *Software-Engineering* (Department of Software Technology) and *Prozeßautomatisierung* (Department of Automation), see [209]. Overall costs approx. 3.2 Mio.ATS.
- Building up the “Informatik-Labor f”ur Prozeßautomatisierung und Embedded Systems” (1999–2000); total cost about 2.1 Mio.ATS.
- Definition, proposal and coordination of Uni-Infrastruktur III projekt “Networked Embedded Systems Research Cluster” (2005-2007); granted funding EUR 488.000,–
- Coordination and planning of renewal of the mandatory labs for Technische Informatik (2005-2006); total costs approx. EUR 350.000,–.
- Definition and proposal for Uni-Infrastruktur IV projekt RES [157] (2007); granted funding approx. EUR 2.050.000,–. Inter-faculty initiative (Informatik, Electrical Engineering, Physics) for establishing a new professorship “Computer-Aided Verification” und infrastructure for experimental evaluation of robust embedded systems.

Research Management

- Project proposal and management FWF-project P6477P (1987–1988, project head: Helmut Prodinger, Department of Algebra und Discrete Mathematics), funding approx. 0.4 Mio.ATS.
- Project proposal and management FWF-Projekt *Versatile Timing Analyzer* (VTA, P8390-TEC, 1991–1995) [221, 213], overall funding approx. 1.9 Mio.ATS.
- Project proposal and management FWF/START-project *Synchronized Universal Time Coordinated for Distributed Real-Time Systems* (SynUTC, P10244-ÖMA, 1995–now) [212, 188], overall funding approx. 6 Mio.ATS. Joint project with Department of Computer Technology (TU Wien) and Institute of General Electrical Engineering and Electronics (TU Wien).
- Project proposal and management FWF/START-project *Sequenced Synchronized Clock Message Protocol/Wireline/Wireless Factory/Facility Fieldbus* (SSCMP/W2F, 1997–2004) [210, 205, 188], overall funding approx. 7 Mio.ATS.
- Project proposal and management project *Prototypenentwicklung f”ur SynUTC* (BMWV Auftragsforschung GZ. 601.577/2-IV/B/9/96 + OeNB “Jubil”aumsfonds”-Projekt 6454, 1997–1998), overall funding approx. 0.55 Mio.ATS. Joint project with Department of General Electrotechnical Engineering and Electronics (TU-Wien).
- Project proposal and management project *Distributed Embedded Systems under OSE* (2000–2001) [191]. Internal project of TU-Wien, overall funding approx. 1.5 Mio.ATS.
- Participation in proposal setup, consortium agreement negotiation and internal setup + supervision EU FP-6 Integrated Project *Automated proof-based System and Software Engineering for Real-Time systems* (ASSERT, IST-004033, 2004–2006) [21]. Collaboration with INRIA Rocquencourt, EADS, Dassault Aviation, Alcatel Space etc.; Coordinator European Space Agency. Total costs 15 Mio.EUR, funding TU approx. EUR 220.000,–.

- Project proposal and supervision BM:VIT FIT-IT-Project *Seamless Campus: Distance Labs* (SC-DL, Proj.No. 808210, 2004-2006). Embedded Systems accompanying measures project, funding EUR 350.000,-.
- Supervision BM:VIT FIT-IT-Project *Distributed Computing in the Presence of Bounded Asynchrony* (DCBA, Proj.No. 808198, 2004). Embedded Systems PhD project (Josef Widder), funding EUR 63.000,-.
- Project proposal and management FWF-project *Asynchronous Distributed Algorithms in the Θ -Model* (THETA, P17757, 2005–2009) [175, 155], overall funding approx. EUR 190.000,-.
- Project definition and proposal setup (jointly with A. Steininger und G. Fuchs) BM:VIT FIT-IT project *Distributed Algorithms for Robust Tick Synchronization* (DARTS, proj.no. 809456, 2005-2008, project head A. Steininger) [168]. Joint project with Austrian Aerospace, total costs EUR 700.000,-. Best project award at the 4th FIT-IT Embedded Systems call.
- Project definition and proposal setup FWF-project *Fault-Tolerant Distributed Algorithms in Sparse Ad Hoc Wireless Networks* (SPAWN, Proj.Nr. P18264, 2005–2009, project head Bettina Weiss) [169], overall funding approx. EUR 185.000,-.
- Supervision BM:VIT FIT-IT project *Transient Fault-Tolerance* (TRAFT, Proj.No. 812205, 2006–2010). Embedded Systems PhD project (Martin Biely), funding EUR 72.000,-.
- Supervision BM:VIT FIT-IT project *Fault-Injection in Distributed Systems* (FIDIS, Proj.Nr. 813441, 2007–2010). Embedded Systems PhD project (Christian Trödhandl), funding EUR 72.000,-.
- Supervision BM:VIT FIT-IT project *Fault-Models for Engineering* (FAME, Proj.Nr. 816454, 2008-2011., project head Bettina Weiss). Embedded Systems PhD projekt (Günther Gridling), funding EUR 72.000,-.
- Project proposal and management FWF projekt *Partially Synchronous Distributed Real-Time Systems*(PSRTS, proj.no. P20529, 2008–2013) [156], total funding EUR 310.000,-.
- Project definition and proposal setup (with A. Steininger and H. Zimmermann) FWF-Projekt *Fault-Tolerant Asynchronous Logic* (FATAL, proj.no. P21694, 2009–now) [154], total funding EUR 451.000,-. Joint project with Institute of Electrical Measurements and Circuit Design and TU Wien's Atominstitut.
- Collaborative project definition and proposal writing (jointly with R. Bloem/TU-Graz, T. Henzinger, K. Chatterjee/IST Austria, A. Biere/Uni Linz, Ch. Kirsch/Uni Salzburg, L. Kovacs, H. Veith, U. Egly/TU Wien) National Research Network *Rigorous Systems Engineering* (RiSE, Austrian Science Fund FWF Proj.Nr. S11405-N23, 2011-now), Sub-Projekt *Reconciling Distributed Computing and Real-Time Systems*, PP05 funding EUR 284.000,-.
Project definition and proposal writing 2nd phase of RiSE NFN, (SHiNE, FWF proj.no. S11405-N23, 2015–now). Continuation of sub-project PP05, jointly with E. Bartocci (sub-task leader); PP05 funding EUR 465.220,-.
- Project definition and proposal setup (jointly with M. Függer) FWF project *Self-stabilizing Byzantine Fault-Tolerant Distributed Algorithms for Integrated Circuits* (SIC, proj.no. P26436, project head M. Függer, 2013–now) [147], total funding EUR 349.000,-.
- Project definition and proposal setup (jointly with A. Steininger und H. Zimmermann) FWF project *Accelerator-based Experimental Analysis and Simulation Modeling of Single-Event Transients in VLSI Circuits* (EASET, proj.no. P26435, project head A. Steininger, 2014–lfd.) [148], total funding EUR 443.000,-. Joint project with Institute of Electrical Measurements and Circuit Design at TU Wien.
- Project definition and proposal writing FWF project *Gracefully Degrading Agreement in Directed Dynamic Networks* (ADynNet, proj.no. P28182, 2016–now) [141], total funding EUR 349.755,-.

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Presentations

1. *Some Investigations Concerning Scheduling in Real-Time Systems*, INRIA Rocquencourt, France, 1989. (Invited)
2. *Monitoring in verteilten Echtzeitsystemen*, Echtzeit'91, Sindelfingen, Germany, 1991.
3. *The Average CRI-Length of a Tree Collision Resolution Algorithm in Presence of Multiplicity-Dependent Capture Effects*, ICALP'92, Vienna, 1992.
4. *The Role of Standards in Real-Time Computing*, NATO ASI on Real-Time Computing, Sint Maarten, 1992.
5. *Monitoring Distributed Real-Time Systems*, NATO ASI on Real-Time Computing, Sint Maarten, 1992.
6. *A Versatile Monitoring System for Distributed Real-Time Systems*, Safecomp'92, Zürich, 1992.
7. *On Random-Trees Arising in the Analysis of Scheduling Algorithms for Real-Time Systems*, Dagstuhl-Seminar 9328 on “Average Case Analysis of Algorithms”, Germany, July 1993. (Invited)
8. *Synchronized UTC for Distributed Real-Time Systems*, Workshop on Real-Time Programming WRTP'94, Lake Reichenau/Germany, 1994.
9. *“Echtzeit”-Systeme* (Habilitationvortrag), Technische Universität Wien, 1995.
10. *Interval-Based Clock Synchronization*, Dagstuhl-Seminar 9611 “Time Services”, Germany, March 1996. (Invited)
11. *Introduction to Project SynUTC*, SynUTC-Workshop, July 1997, Technische Universität Wien.
12. *Interval-based Clock Synchronization*, SynUTC-Workshop, July 1997, Technische Universität Wien.
13. *Challenges in Interval-based Clock Synchronization*, Dagstuhl-Seminar 9728 on “Average Case Analysis of Algorithms”, Germany, July 1997. (Invited)
14. *Internet-Based Real-Time Computing (Panel Discussion on Real-Time Systems)*, 22nd Annual International Computer Software & Applications Conference COMPSAC'98, August 1998, Vienna, Austria. (Invited)
15. *Experimental Evaluation of High-Accuracy Time Distribution in a COTS-based Ethernet LAN*, 24th IFAC/IFIP Workshop on Real-Time Programming WRTP'99, Schloß Dagstuhl, Germany, May/June 1999.
16. *High-Accuracy Time Services and Fault-Tolerant Clock Synchronization*, 37th IFIP WG10.4 Annual Meeting (Workshop on “Time and Dependability”), Martinique, France, January 2000. (Invited)
17. *Applied Research: A Scientist's Perspective*, Keynote speech at joint 25th IFAC/IFIP Workshop on Real-Time Programming (WRTP'00) and Workshop on Algorithms and Architectures for Real-Time Control (AARTC'00), Mallorca, Spain, May 2000. (Invited)

18. *3 Years of START Project Y41-MAT*, Presentation for the International Jury, Austrian Science Foundation (FWF), Vienna, June 17, 2000.
19. *Embedded Systems*, Presentation at BM:vit working group meeting “IT-Strategy 2000”, Oesterreichische Computer Gesellschaft OCG, August 3, 2000.
20. *How to model link failures: A perception-based fault model*, International Conference on Dependable Systems and Networks (DSN’01), Göteborg, Sweden, July 1–4, 2001.
21. *Ein “Versuch über die wahre Art, das Clavier zu spielen”*, Berufungsvortrag Embedded Computing Systems, TU Wien, Vienna (Austria), December 18, 2001.
22. *Formally verified byzantine agreement in presence of link faults*, 22nd International Conference on Distributed Computer Systems (ICDCS’02), July 2002, Vienna, Austria.
23. *Forschungsschwerpunkt Technische Informatik*, Kick-Off-Event Informatik-Netzwerk IN:N der TU-Wien, Vienna, Austria, 30. September 2002.
24. *Hybrid Process and Link Failures in Synchronous, Partially Synchronous and Asynchronous System Models*, Faculty of Computer Science, University of Lisboa, 28. Jänner 2003
25. *Randomized Asynchronous Consensus with Imperfect Communications*, 22nd Symposium on Reliable Distributed Systems (SRDS’03), Florence, Italy, October 6–8, 2003
26. *2004 Research Topics*, Embedded Computing Systems Group E182/2, TU-Wien, 17. Oktober 2003
27. *Embedded Systems an der TU-Wien*, FIT-IT Workshop 2003, Siemens, Wien, 17. Jänner 2003
28. *Asynchronous Distributed Real-Time Systems? An Overview of Future ECS Research*, Institut für Technischen Informatik, TU-Wien, 20. März 2003
29. *Institut für Technische Informatik: Embedded Computing Systems Group*, Institut für Technischen Informatik, TU-Wien, 29. September 2003
30. *The Θ -Model*, INRIA Rocquencourt, Versailles, 3. September 2004
31. *The Θ -Model*, 2. ASSERT RC/SF-Meeting, TU-Vienna, 20. September 2004
32. *The Θ -Model*, Diskussionskreis Fehlertoleranz (DFT’04), Humboldt-Universität Berlin, 12. November 2004
33. *IKT in Österreich 2006: Wissenschaftliche Forschung - Quo vadis?*, BM:vit Tagung IKT Forschung Österreich: Herausforderung, Chancen und Positionierung, Wien, Palais Strudlhof, 5.–6. Dezember 2006. (Invited)
34. *Keynote: A Perspective of Fault-Tolerant Clock Synchronization*, International IEEE Symposium on Precision Clock Synchronization for Measurement, Control and Communication (ISPCS’07), October 1-3, 2007, Austrian Academy of Sciences, Vienna, Austria. (Invited Keynote)
35. *Distributed Algorithms and VLSI — An Appetizer*, Dagstuhl-Seminar 08371 on “Distributed Algorithms on VLSI Chips” (Organizers: Bernadette Charron-Bost, Jo Ebergen, Shlomi Dolev, Ulrich Schmid), SchloßDagstuhl, Germany, September 7–10, 2008.
36. *Challenges in Fault-Tolerant Distributed Real-Time Systems*, RiSE Workshop, TU Graz, January 22, 2010.
37. *Reconciling Distributed and Real-Time Computing*, RiSE Hearing, Austrian Science Foundation (FWF), Vienna, July 2, 2010.
38. *Invited Tutorial: Synchrony and Time in Fault-tolerant Distributed Algorithms*, Formal Modeling and Analysis of Times Systems Conference (FORMATS’10), IST Austria, September 8–10, 2010. (Invited Tutorial) Tutorial
39. *Distributed Algorithms*, Joint VCLA/RiSE Winter School on Verification, February 6-10, 2012, Vienna.
40. *Technische Informatik an der TU Wien*, HTL St. Pölten, May 2012.
41. *Technische Informatik Universitätsstudium und HTL Ausbildung: Chancen und Herausforderungen*, Fachwissenschaftliches Koordinationsseminar der Pädagogischen Hochschule für NÖ, HTBLuVA Salzburg, December 2012.
42. *Fault-Tolerant Distributed Algorithms*, RiSE Winter School on Verification, February 11-15, 2013, Vienna.
43. *Parameterized Verification Challenges in Distributed Algorithm*, RiSE Workshop, November 19, 2013, Vienna.
44. *Easy Impossibility Proofs for k -Set Agreement*, Dagstuhl-Seminar 16282 on *Topological Methods in Distributed Computing*, July 10–15, 2016, Schloss Dagstuhl–Leibniz-Zentrum fuer Informatik.
45. *Reconciling Fault-Tolerance and Robustness ?*, Workshop on Design and Analysis of Robust Systems @ CPS-Week 2016, Hofburg, Vienna, Austria, April 11, 2016. (Invited talk)