Faiq KHALID

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Education

- PhD in Electrical Engineering (**2017 - Present)**
  Vienna University of Technology (TU Wien)
  Department of Computer Engineering
- Masters in Electronics Engineering (**2014 - 2016)**
  National University of Sciences & Technology (NUST)
  School of Electrical Engineering and Computer Sciences (SEECS), Islamabad, Pakistan
  CGPA: **3.75/4.00**

Work Experience

Research

1. Project Assistant from **11th May 2017** till **Present** in **Computer Architecture and Robust Energy-Efficient Technologies (CARE-Tech.) at** the Embedded Computing Systems Group, Institute of Computer Engineering, Faculty of Informatics, Vienna University of Technology (TU Wien), under the supervision of **Prof. Dr. Muhammad Shafique**.
2. Research Assistant from **1st November 2009** till **30th April 2017** at **System Analysis and Verification** (SAVE: A Research Lab in NUST SEECS) Islamabad, Pakistan, under the supervision of **Dr. Osman Hasan**.
3. Research Internee from **1st December 2016** to **31st December 2016** at **Chair for Embedded Systems (CES)** under the supervision of **Prof. Dr. Joerg Henkel** in Karlsruhe Institute of Technology (KIT), Karlsruhe, Germany.
4. Research Internee from **16th April 2016** to **4th May 2016** at **Chair for Embedded Systems (CES)** under the supervision of **Prof. Dr. Joerg Henkel** in Karlsruhe Institute of Technology (KIT), Karlsruhe, Germany.
5. **General Co. Chair and Web Coordinator** in **Workshop on System Analysis and Verification (WSAV-2016)** held at NUST School of Electrical Engineering and Computer Sciences (SEECS), Islamabad, Pakistan
6. Summer Internship from **9th August 2010** to **11th September 2010**, in **Hybrid Solid State** Project (a research-based project undertaken by NUST in collaboration with SWAF and DTS Japan) in SEECS, NUST, Islamabad, Pakistan**.**

Conference Management

1. **General Co-Chair**, Workshop on System Analysis and Verification (WSAV), 2016
2. **Web Coordinator**, Workshop on System Analysis and Verification (WSAV), 2016
3. **Technical Program Committee**, ICT for Electronics of Frontiers of Information Technology (FIT), 2015

Teaching

4. Teaching Assistant for "**Analog Integrated Circuit Design**" in PG Semester **Spring 2016**.
5. Teaching Assistant for "**VLSI Design**" in UG Semester **Spring 2016**.
6. Teaching Assistant for "**Advanced Digital VLSI Design**" in PG Semester **Spring 2016**.
7. Teaching Assistant for "**Advanced Digital System Design**" in PG Semester **Fall 2015**.
8. Teaching Assistant for "**Embedded System Design**" in UG Semester **Fall 2011.**
9. Teaching Assistant for "**Embedded System Design**" in UG Semester **Spring 2011**.
10. Teaching Assistant for "**VLSI Design**" in UG Semester Spring **Fall 2011**.
11. Teaching Assistant for "**Digital Logic Design**" in UG Semester **Spring 2010**.

Professional and Skills Development Experiences

1. I have attended a **Workshop on Solar Energy Conversion Systems** held on 5th January 2011 at SEECS, NUST, Islamabad, Pakistan**.**
2. I have participated in **NVS Semester Project Exhibition-SPEX'10** held on 15th June 2010 at SEECS, NUST, Islamabad, Pakistan**.**
3. I have presented a research paper in **International Conference on Information and Emerging Technologies (ICIET) 2010** held at National University of Computer and Emerging Sciences, Karachi, Pakistan.
4. I have participated in **Workshop on Introduction of RF Microelectronics** held on 2nd August to 6th August 2010 at SEECS, NUST, Islamabad, Pakistan**.**
5. I have participated in **Workshop on Sigma Delta ADC's Design** held on 26th to 30th July 2010 at SEECS, NUST, Islamabad, Pakistan**.**
6. I have participated in **Workshop on Cadence based IC Design** held on 19th to 23rd July 2010 at SEECS, NUST, Islamabad, Pakistan**.**
7. I have participated in **Workshop on Operational Amplifier** held on 12th to 17th July 2010 at SEECS, NUST, Islamabad, Pakistan**.**
8. I have worked as Organizing Committee Member of One-Day **Workshop on From Ideas to Assets: Investing Wisely in Intellectual Capital** held on 8th May 2009 at NUST SEECS.
9. I have attended a **Workshop on 3D Studio Max** held on 5th January 2009 at NUST SEECS.

Publications

Refereed Journals

[J1]. S. Iqbal, M. U. Sardar, **F. Khalid**, O. Hasan, "Statistical Model Checking of Relief Supply Location and Distribution in Natural Disaster Management", International Journal of Disaster Risk Reduction, 2018, (Accepted in April)

[J2]. **F. Khalid**, S. R. Hasan, O. Hasan and F. Awwad, "Runtime Hardware Trojan Monitors Through Modeling Burst Mode Communication Using Formal Verification", in Integration the VLSI Journal, Volume 61, Issue C, pp. 62-76, Elsevier, 2018.

[J3]. S. A. A. Bukhari, **F. Khalid**, O. Hasan, M. Shafique and J. Henkel, *"FAMe-TM: Formal Analysis Methodology for Task Migration Algorithms in Many-Core Systems"*, in Science of Computer Programming, Elsevier, Vol. 133, Part 2, 2017, pp. 154-174.

[J4]. **F. Khalid**, S. R. Hasan, O. Hasan, and F. Awwad, *"Analyzing Vulnerability of Asynchronous Pipeline to Soft Errors: Leveraging Formal Verification"*, in Journal of Electronic Testing: Theory and Applications, Volume 32, Issue 5, Springer 2016, pp. 569-586.

[J5]. **F. Khalid**, S.R. Hasan, N. Sharif, N. Ramzan and O. Hasan, "*Timing Variation Aware Dynamic Digital Phase Detector for Low Latency Clock Domain Crossing",* in IET Circuits, Devices & Systems, 2014, Volume 8, Issue 1, pp. 58-64.

Peer Reviewed Conferences

[C1]. **F. Khalid**, S. Nanjiani, S. R. Hasan, O. Hasan, F. Awwad and M. Shafique, "*Low Power Digital Clock Multipliers for Battery-Operated Internet of Things (IoT) Devices*", International Symposium on Circuits and Systems (ISCAS 2018), Florence, Italy (To Appear).

[C2]. M. Hailesellasie, S. R. Hasan **F. Khalid**, F. Awwad and M. Shafique, "*FPGA-Based Convolutional Neural Network Architecture with Reduced Parameter Requirements*", International Symposium on Circuits and Systems (ISCAS 2018), Florence, Italy (To Appear).

[C3]. S. Khan, **F. Khalid**, O. Hasan and J. M. Cardoso, "*Formal Verification of A Domain Specific Language for Run-time Adaptation*", IEEE International Systems Conference (SysCon 2018), Vancouver, British Columbia, Canada (To Appear).

[C4]. M. Shafique, T. Theocharides, C. S. Bouganis, M. Abdullah Hanif, **F. Khalid**, R. Hafiz, S. Rehman, "*An Overview of Next-Generation Architectures for Machine Learning: Roadmap, Opportunities and Challenges in the IoT Era*", Special Session, in Design, Automation and Test in Europe (DATE-2018), To Appear.

[C5]. **F. Khalid**, S. R. Hasan, O. Hasan and F. Awwad, "*Behavior Profiling of Power Distribution Networks for Runtime Hardware Trojan Detection*", in International Midwest Symposium on Circuits and Systems (MWSCAS 2017), IEEE Circuit and System Society (CAS), Boston, MA, USA, pp. 1316 -1319.

[C6]. **F. Khalid,** O. Hasan, S. R. Hasan and F. Awwad, "*Power Profiling of Instructions of Microcontroller to Detect Hardware Trojans without Golden Circuit Models*", Design, Automation & Test in Europe (DATE-2017), Laussane, Switzerland, pp. 294 - 297.

[C7]. S. A. A. Bukhari, **F. Khalid**, O. Hasan, M. Shafique and J. Henkel, "*CAnDy-TM: Comparative Analysis of Dynamic Thermal Management in Many-Cores using Model Checking*", in Design, Automation & Test in Europe (DATE-2017), Laussane, Switzerland, pp. 1289 - 1292.

[C8]. I. Abbasi, **F. Khalid**, A. Kamboh, O. Hasan, *"Formal Verification of Gate-Level Multiple Side Channel Parameters to detect Hardware Trojans"*, in Formal Techniques for Safety-Critical Systems (FTSCS 2016), Tokyo, Japan, pp. 75 - 92.

[C9]. W. Gul, S. R. Hasan, O. Hasan, **F. Khalid** and F. Awwad, "*Synchronously Triggered GALS Design Templates Leveraging QDI Asynchronous Interfaces,*" in IEEE Symposium on Circuits and System (ISCAS 2016), Jun. 2016, pp. 2615-2618.

[C10]. **F. Khalid**, I. Abbasi, F. Khalid, O. Hasan, S. R. Hasan and F. Awwad, "*A Self-Learning Framework to Detect the Intruded Integrated Circuits,*" in IEEE Symposium on Circuits and System (ISCAS 2016), Jun. 2016, pp. 1702-1705.

[C11]. **F. Khalid**, O. Hasan, S. R. Hasan and F. Awwad, "*Formal Analysis of Macro Synchronous Micro Asynchronous Pipeline for Hardware Trojan Detection,*" in Nordic Circuits and Systems Conference (NORCAS 2015): NORCHIP & International Symposium on System-on-Chip (SoC), Oct. 2015, pp.1- 4.

[C12]. S. A. A. Bukhari, **F. Khalid**, O. Hasan, M. Shafique and J. Henkel, "*Formal Verification of Distributed Task Migration for Thermal Management in On-chip Multi-Core Systems using nuXmv*", in Formal Techniques for Safety-Critical Systems (FTSCS 2014), Luxembourg City, Luxembourg, 2014, pp 32 - 46.

[C13]. **F. Khalid**, O. Hasan, S. R. Hasan and F. Awwad, "*Hardware Trojan detection in soft error tolerant macro synchronous micro asynchronous (MSMA) pipeline*", in IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 2014), Aug. 2014, pp. 659 - 662.

[C14]. **F. Khalid**, O. Hasan, S. R. Hasan and F. Awwad, "*Low Power Soft Error Tolerant Macro Synchronous Micro Asynchronous (MSMA) Pipeline*," in IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2014), July 2014, pp. 601 - 606.

[C15]. **F. Khalid**, O. Hasan, S. R. Hasan and F. Awwad, "*Modified Null Convention Logic Pipeline to Detect Soft Errors in Both Null and Data Phase,*" in IEEE International Midwest Symposium on Circuits and Systems (MWCAS 2012), IEEE Circuit and System Society (CAS), Boise, Idaho, USA, August 2012, pp. 402 - 405.

[C16]. **F. Khalid**, N. Sharif, N. Ramzan, O. Hasan and S.R. Hasan. "*Quantitative Analysis of State-of-the-Art Synchronizers: Clock Domain Crossing Perspective",* in IEEE International Conference on Emerging Technologies (ICET-11), Islamabad, Pakistan, September 2011, pp. 1 - 6.

[C17]. **F. Khalid**, N. Ramzan and O. Hasan, "*Towards Precise, Scalable and Automatic Analysis of Analog and Mixed-Signal Circuits",* in IEEE International Conference on Information and Emerging Technologies (ICIET-10), Karachi, Pakistan, June 2010, pp. 1 - 6.

Book Chapters

[B1]. I. Abbasi, **F. Khalid**, A. Kamboh, O. Hasan, "*Formal Verification of Gate-Level Multiple Side Channel Parameters to detect Hardware Trojans*", Formal Techniques for Safety-Critical Systems, 2016, pp 75-92.

[B2]. S. A. A. Bukhari, **F. Khalid**, O. Hasan, M. Shafique and J. Henkel, "*Formal Verification of Distributed Task Migration for Thermal Management in On-chip Multi-Core Systems using nuXmv*", Formal Techniques for Safety-Critical Systems, 2014, pp 32-46.

Technical Reports

[T1]. S.A.A. Bukhari, **F. Khalid** and O. Hasan, "*Formal Verification of Distributed Task Migration for Thermal Management in On-chip Multi-Core Systems using nuXmv*", Technical Report, NUST, Islamabad, Pakistan, 2014.

External Reviewers/Sub-reviewer

Refereed Journals

1. IEEE Transactions on Very Large Scale Integrated, 2016, 2017
2. IEEE Transactions on Circuits and Systems II, 2016
3. IEEE Transactions on Circuits and Systems I, 2016
4. IEEE Transactions on Computer-Aided Design, 2016, 2017, 2018
5. IEEE Transactions on Computers, 2017
6. IEEE Electronics Letter, 2016
7. IEEE Embedded System Letter, 2017
8. IEEE Sensors Journal, 2017
9. IEEE Software, 2017
10. Journal of Signal Processing Systems, 2017
11. Frontiers of IT & Electronic Engineering Application-Aware Energy and Throughput Optimization in Multicore Processors, 2017
12. ACM Computing Surveys, 2018

Peer Reviewed Conferences

1. Computing Frontiers, 2018
2. IEEE International Conference on Design & Technology of Integrated Systems in Nanoscale Era, 2018
3. IEEE/ACM Design, Automation & Test in Europe Conference & Exhibition, 2018
4. International Workshop on Optimization of Energy Efficient HPC & Distributed Systems, 2018
5. International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation, 2018
6. IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, 2017
7. IEEE/ACM Symposium on Embedded Systems for Real-Time Multimedia, 2017
8. Forum on specification & Design Languages, 2017
9. International Conference on Field-Programmable Logic and Applications, 2017, 2018
10. International Symposium on Circuits and Systems, 2017, 2018
11. International Green and Sustainable Computing Conference, 2017
12. International Symposium on Power and Timing Modeling, Optimization and Simulation, 2017
13. International Conference on Embedded Computer System: Architectures, Modeling and Simulations, 2017
14. International Conference on VLSI Design, 2017
15. IFIP/IEEE International Conference on Very Large Scale Integration, 2017
16. International Conference on Compilers, Architecture, and Synthesis for Embedded Systems, 2017
17. IEEE International Midwest Symposium on Circuits and Systems, 2016, 2017
18. IEEE International New Circuits and Systems Conference, 2016, 2017
19. IEEE International Conference on Open Source Systems & Technologies, 2016
20. IEEE International Conference on Computer Engineering and Systems, 2014, 2015, 2016
21. IEEE International Conference on Innovations in Information Technology, 2012
22. IEEE Canadian Conference on Electrical and Computer Engineering, 2012
23. IEEE International Conference on Microelectronics, 2015
24. IEEE Frontiers of Information Technology, 2014, 2015, 2017
25. IEEE International Multi Topic Conference, INMIC-2014

Technical skills

Over the years I have engaged in various research projects. Thus, I have developed hand-on expertise in:

- Synopsys based ASIC designing
- CADANCE based ASIC designing
- Model Checking (nuXmv)
- Mathematical Modeling of AMS circuits in CAS, PSpice
- Hardware Descriptive Languages, i.e., Verilog A, Verilog HDL and VHDL and PSL
- Programming in MATLAB
- LATEX, Miktex
- Programming in MAXIMA (Computer Algebra System)
- Programming in C/ C++

Projects

Research Projects

1. **IoT4CPS: Trustworthy IoT for CPS (A Flagship Project from FFG (Austrian Funding Agency))**
   In this project, I am working as a project assistant at TU Wien, which is one of the consortium members of IoT4CPS project, under the supervisions of Prof. Dr. Muhammad Shafique. In this project, my responsibilities are: to develop the methodologies for robust communication protocols and data analysis algorithms for IoT based CPS systems.
2. **Vulnerability Analysis of Asynchronous Pipeline**
   In this project, we propose a framework to analyze the robustness of asynchronous pipelines by identifying and formally analyzing the vulnerable paths/nodes/block using the nuXmv model checker.
3. **A Self-Learning Framework to Detect the Abnormal Integrated Circuits**
   In this project, we combine the delay-based signature extraction mechanism with machine learning algorithms to develop a self–learning framework that can detect the abnormal integrated circuits.
4. **Formal Analysis of Macro Synchronous Micro Asynchronous to Ensure the Robustness**
   In this project, we propose to use a model checker, i.e., nuXmv, to detect the vulnerable paths in the MSMA pipeline to analyze and detect the abnormal behavior.

5. **Design for Robust Soft Error Tolerant Macro Synchronous Micro Asynchronous (MSMA) Pipeline**
   The main idea is to accommodate asynchronous standard cells within the synchronous pipeline and thus giving rise to a macro synchronous micro asynchronous (MSMA) pipeline. Therefore, in this project, we embed the delay based signature technique in MSMA pipeline to identify the abnormalities.
6. **Low Power Soft Error Tolerant Macro Synchronous Micro Asynchronous (MSMA)Pipeline**
   In this project, we propose a low power and soft error tolerant solution for synchronous systems (MSMA) that leverages the asynchronous pipeline within a synchronous framework.
7. **Modified Null Convention Logic Pipeline to Detect Soft Errors in Both Null and Data Phase**
   This technique provides a modified approach to overcome the limitations of fault propagation and SE in NULL cycle with, on average, comparable power and latency costs.
8. **Development of a tool for precise and scalable analysis of AMS circuits (Using MAXIMA)**
   This tool is a computer algebra system based analyzer for AMS designs. The distinguishing features that make it the best choice for AMS circuit analysis include the manipulation of symbolic and numerical expressions, including differentiation, integration, ordinary differential equations (ODEs), systems of linear equations etc.

Master Thesis

1. **Runtime Monitors to Ensure the Robustness of Burst Mode Communication**
   In this project, we proposed a generic framework, which leverages the burst mode communication protocol, to design a robust burst mode communication.

BEE Final Year Project

1. **Design of Digital Phase Detectors for Cross Clock Domains**
   This project intends to provide a safe solution for crossing data between multiple clock domains. The solution consists of a Digital Phase Detector (DPD) that estimates phase variations between clock domains by utilizing prior knowledge of the frequency ratios to develop sampling criteria. An algorithm is developed to analyze the sampled information that will help in deciding a particular phase among the given phases of the local clock closest to the remote clock phase. The most important and distinguishing feature of the proposed architecture is its ability to achieve a low latency.

Honors / Awards achieved

1. 2018: Richard Newton Young Fellow Award at DAC
2. 2014: Best Researcher of SAVe lab
3. 2009: 1st Position in NUST Olympiad for Circuits Design and Speed Wiring
4. 2006: 2nd position in JAZZ Intra-College General Knowledge Quiz Competition
5. 2004: 2nd position in Inter-District Science Quiz Competition
6. 2004: 4th position in Faisalabad Board in Matriculation
7. 2004: Quaid-e-Azam Medal in Matriculation
8. 2003: 2nd Position in Inter-District Science Quiz competition

Community Involvement

1. Participated as a volunteer for E-village Project (A social welfare project of SEECS-PSA)
2. Work for BEE Society as a volunteer.

Hobbies and Interests

Cricket, Football, Table Tennis and Web designing

References

Asst. Prof. Dr. Osman Hasan
National University of Sciences and Technology
Islamabad, Pakistan.
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Asst. Prof. Dr. Syed Rafay Hasan
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Prof. Dr. Muhammad Shafique
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