Dipl.-Ing. Dipl.-Ing. Jürgen Maier, BSc

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Personal Data

Nationality	Austria
Memberships	IEEE
Languages	German(native), English
Interests	Chief of Voluntary Fire Brigade Languages: currently Russian Sports: Beachvolleyball, Basketball, Football

Education

2015/10 - present **Doctoral programme in Computer Sciences at TU Wien, Vienna, Austria**

2013/10 - 2016/04 **Master's programme Microelectronics and Photonics graduated with distinction, TU Wien, Vienna, Austria**
Masterthesis "Modeling III-V Semiconductor Interfaces at an Atomistic Level using Empirical Potentials"

2011/09 - 2014/10 **Master's programme Computer Engineering graduated with distinction, TU Wien, Vienna, Austria**
Masterthesis "Online Test Vector Insertion – A Concurrent Built-In Self-Testing (CBIST) Approach for Asynchronous Logic"

2008/10 - 2011/09 **Bachelor's programme Computer Engineering graduated with distinction, TU Wien, Vienna, Austria**
Bachelorthesis "Powerline in Building Automation"

2005/07 **HTL Donaustadt, 1220 Vienna**
Departement for Electronic Data Processing and Organisation

Employment

2018/01 - present **TU Wien, Vienna, Austria**
Institute of Computer Engineering, Embedded Computing Systems Group
University Assistant

2015/09 - present **TU Wien, Vienna, Austria**
Institute of Computer Engineering, Embedded Computing Systems Group
Project Assistant

2014/01 - 2015/02 **TU Wien, Vienna, Austria**
Institute of Energy Systems and Electrical Drives, Energy Economics Group (EEG), Project Employee

2006/10 - 2010/12 **CSPmed GmbH., later Compugroup AG, Vienna, Austria**
Programming and Support

2006/01 - 2006/07 **Military Service in Mistelbach, Austria**

Awards and Scholarships

2019/02	Christiana Hoerbiger Scholarship, TU Wien, Vienna, Austria
2016/05	Excellence Scholarship, Windhag foundation for Lower Austria, Austria
2014/12	Nominee for "Distinguished Young Alumna/Alumnus"-Award, Faculty of Informatics, TU Wien
2014/11	Excellence Scholarship, Faculty of Electrical Engineering and Information Technology, TU Wien
2014/04	Best paper award at the 17th International Symposium on Design and Diagnostics of Electronic Circuits Systems, Warsaw, Poland
2013/11	Excellence Scholarship, Faculty of Informatics, TU Wien
2012/11	Excellence Scholarship, Faculty of Informatics, TU Wien
2011/12	Excellence Scholarship, Faculty of Informatics, TU Wien

Publications

[1] J. Maier, M. Függer, T. Nowak, and U. Schmid. "Transistor-Level Analysis of Dynamic Delay Models". In: accepted for ASYNC'19. 2019.

[2] J. Maier and A. Steininger. "Efficient Metastability Characterization for Schmitt-Triggers". In: accepted for ASYNC'19. 2019.

[3] Chuchu Fan, Yu Meng, Jürgen Maier, Ezio Bartocci, Sayan Mitra, and Ulrich Schmid. "Verifying nonlinear analog and mixed-signal circuits with inputs". In: *IFAC-PapersOnLine* 51.16 (2018). 6th IFAC Conference on Analysis and Design of Hybrid Systems ADHS 2018, pp. 241–246. ISSN: 2405-8963. DOI: 10.1016/j.ifacol.2018.08.041. URL: http://www.sciencedirect.com/science/article/pii/S2405896318311571.

[4] M. Függer, J. Maier, R. Najvirt, T. Nowak, and U. Schmid. "A faithful binary circuit model with adversarial noise". In: *2018 Design, Automation Test in Europe Conference Exhibition (DATE)*. Nominee for Best Paper Award. Mar. 2018, pp. 1327–1332. DOI: 10.23919/DATE.2018.8342219. URL: https://ieeexplore.ieee.org/document/8342219/.

[5] Jürgen Maier. *Modeling the CMOS Inverter using Hybrid Systems*. Tech. rep. TUW-259633. E182 - Institut für Technische Informatik; Technische Universität Wien, 2017. URL: http://publik.tuwien.ac.at/files/publik_259633.pdf.

[6] Jürgen Maier and Hermann Detz. "Atomistic modeling of interfaces in III-V semiconductor superlattices". In: *physica status solidi (b)* 253.4 (2016), pp. 613–622. ISSN: 1521-3951. DOI: 10.1002/pssb.201552496. URL: http://dx.doi.org/10.1002/pssb.201552496.

[7] A. Steininger, J. Maier, and R. Najvirt. "The Metastable Behavior of a Schmitt-Trigger". In: *2016 22nd IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC)*. May 2016, pp. 57–64. DOI: 10.1109/ASYNC.2016.19. URL: https://ieeexplore.ieee.org/document/7584893/.

[8] A. Steininger, R. Najvirt, and J. Maier. "Does Cascading Schmitt-Trigger Stages Improve the Metastable Behavior?" In: *2016 Euromicro Conference on Digital System Design (DSD)*. Aug. 2016, pp. 372–379. DOI: 10.1109/DSD.2016.56. URL: https://ieeexplore.ieee.org/document/7723576/.

[9] Jürgen Maier. "Modeling III-V Semiconductor Interfaces at an Atomistic Level using Empirical Potentials". Master Thesis, Institute of Solid State Electronics, TU Wien, Vienna, Austria. MA thesis. TU Wien, Vienna, Austria, Apr. 2016. URL: http://catalogplus.tuwien.ac.at/UTW:UTW:UTW_alma2150179390003336.

[10] H. Detz, J. Maier, and G. Strasser. "Atomistic Modeling of Interfacial Strain in III-V Heterostructures". In: *2015 Compound Semiconductor Week*. June 2015, pp. 1–2.

[11] J. Maier, H. Detz, and G. Strasser. "Atomistic Modeling of III-V Semiconductor Interfaces". In: *Vienna Young Scientist Symposium*. June 2015, pp. 38–39.

[12] J. Maier and A. Steininger. "Online Test Vector Insertion: A Concurrent Built-In Self-Testing (CBIST) Approach for Asynchronous Logic". In: *Design and Diagnostics of Electronic Circuits Systems, 17th International Symposium on*. Apr. 2014, pp. 33–38. DOI: 10.1109/DDECS.2014.6868759. URL: https://ieeexplore.ieee.org/document/6868759/.

[13] Jürgen Maier. "Online Test Vector Insertion: A Concurrent Built-In Self-Testing (CBIST) Approach for Asynchronous Logic". Master Thesis, Institute of Computer Engineering, TU Wien, Vienna, Austria. MA thesis. TU Wien, Vienna, Austria, Oct. 2014. URL: http://catalogplus.tuwien.ac.at/UTW:UTW:UTW_alma2139475450003336.

Presentations

5. *A Faithful Binary Circuit Model with Adversarial Noise*, 2018 Design, Automation & Test in Europe (DATE), Dresden, Germany, March 2018.

4. *Involution Model: Faithful Delay Prediction in Digital Circuits*, Université Paris-Sud, Laboratoire de Recherche en Informatique (LRI), Paris, France, July 2017.

3. *Atomistic Interface Modeling in III-V Semiconductor Superlattices*, Joint Annual Meeting of the Austrian Physical Society and the Swiss Physical Society, Vienna, Austria, 2015.

2. *Atomistic Modeling of III-V Semiconductor Interfaces*, Vienna Young Scientists Symposium, Vienna, Austria, 2015.

1. *Online Test Vector Insertion: A Concurrent Built in Self-Testing (CBIST) Approach for Asynchronous Logic*, 17th International Symposium on Design and Diagnostics of Electronic Circuits Systems, Warsaw, Poland, 2014.