“Single-chip Cloud Computer”
A many-core research platform from Intel Labs
Compute evolving to "Tera-Scale"

Performance

TIPS
GIPS
MIPS
KIPS

Dataset Size
Kilobytes
Megabytes
Gigabytes
Terabytes

Text
Multi-media
3D and Video
Model-Based Apps

Single-Core
Multi-Core
Many-core

INTEL
TERA-SCALE
RESEARCH

Entertainment, Learning
Financial Analytics
Personal Media Creation and Management
Health and Medicine

3D and Video
Text
Multi-media
Model-Based Apps

KIPS
MIPS
GIPS
TIPS

Personal Media Creation and Management
Health and Medicine

Many-core
Multi-Core
Single-Core

Terabytes
Gigabytes
Megabytes
Kilobytes

Compute evolving to "Tera-Scale"
Tera-Scale Scaling Challenges

- Energy Efficiency
- Design Complexity
- Programming Models
- Emerging Applications
Single-chip Cloud Computer

- Experimental many-core CPU/Platform for “Tera-Scale” HW/SW research
  - Many-core processor research ➔ Hardware
  - Parallel Programming research ➔ Software
- Research platform shared with industry and academic collaborators to enable/encourage “tera-scale” explorations

Energy Efficiency
- Dynamic voltage/frequency scaling
- 1/3 power reduction for core-core I/O

Design Complexity
- Array of small IA-based tiles could lead to more agile, flexible designs

Programming Model
- Message-passing approach proven to scale to 1000’s processors

Application Development
- Sharing with Microsoft* & others for academic, industry innovation
The SCC Platform

- Debug tools – Memory Reader, SoftRAM, R/W SCC Config Registers
- Provides SW based virtual I/O (e.g. performance widget)
- Konsole w/ SSH connections to all booted cores
- Commandline tools – sccBoot, sccReset, sccBMC, sccKonsole

Intel SCC – a complete HW/SW “Tera-Scale” research platform
A closer look

- 24 Dual-core tiles (48 IA cores)
- 24 Routers
- Mesh network with 256 GB/s bisection bandwidth
- 4 Integrated DDR 3 memory controllers
- 1.3 Billion transistors

Dual-core SCC Tile

- L2 Cache
- Core 1
- Core 2
- Message Buffer
- ROUTER
- Memory Controller
- 1 TILE

[Image of a closer look at the architecture]
Dynamic Power Management

Fine-grain, software-controlled power management
- 8 Voltage and frequency islands ➔ Dynamic range 25-125W
- Each tile can run at a different frequency
- 6 banks of 4 tiles can run at different voltages
- Independent V&F control for I/O network & MCs

48 IA cores at 25-125W
Advancing Parallel SW Research

- The SCC eliminates significant complexity & power by removing hardware cache coherency

- Enables exploration of more scalable alternatives:
  - Message passing models common in datacenter, HPC
  - Software-managed, adaptive cache coherency
SCC Co-Traveler Program

Goal:
Enable Tera-Scale Research by Industry/academic institutions

• Access to SCC System(s), Tools, Documentation, Open Source SW, Support etc
• Access to “Eco-system” of users, Intel sponsored conferences, SCC Workshops
• Working with 100+ partners around the world
• Deployment in waves, currently executing wave #1
SCC Co-Traveling in action

Financial Analytics w/ shared virtual memory

Microsoft Visual Studio

Advanced Power Management

JavaScript Physics Modeling

HPC Parallel Workloads

Hadoop Web Search
# SCC Co-Traveler Timeline (2010)

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- Santa Clara: Feb 12
- Germany: Mar 16
- EWME: May 10-12
- Workshops and Conferences: TBD
- Registration
- Applications
- 15 Apr Deadline
- Notification: 1st Week of May
- Overview, Messaging LIB, EAS, How To Use Linux
- Sample Workflows
- Final Docs, Website Active
- Beta Testers
- General HW Availability
- Datacenter For Remote Access
Summary:

• Many-Core/Tera-Scale compute transition will happen!
• The Intel SCC is an experimental many-core research platform designed to help addressing the “tera-scale” HW and SW challenges:

  - Energy Efficiency
    - Dynamic voltage/frequency scaling
    - 1/3 power reduction for core-core I/O
  - Design Complexity
    - Array of small IA-based tiles could lead to more agile, flexible designs
  - Programming Model
    - Message-passing approach proven to scale to 1000’s processors
  - Application Development
    - Sharing with Microsoft* & others for academic, industry innovation

• Intel is making the SCC available world-wide to enable industry and academic research and innovation.
• Visit our website: www.intel.com/info/scc

• Technical Questions about SCC Platform, Research: SCC_Technical_Questions@intel.com