The Java Virtual Machine in Hardware

An Exercise in HW/SW Partitioning

Martin Schöberl
Areas Covered

- The Java virtual machine (JVM)
  - Bytecode instruction set
  - Internals
  - Implementation issues
- Basic Java processor architectures
- SoC, FPGA design flow
- Java Processor - JOP
Aim of the Course

- Prepare for:
  - Virtual machine design
  - System-on-Chip design with
    - FPGAs and the resulting
    - HW/SW co-design issues

- Prerequisites:
  - Java
  - Basic VHDL (Digitales Design)
Organization

- Blocked
  - Talk
  - Supervised lab
- Small project
  - Group work (up to 4)
  - Short description in a Wiki
    - http://www.jopwiki.com/JvmHW
- Final Presentation
Dates

- Tu 10.3.2009 14:00
- Th 12.3.2009 14:00 1st Lab
- Tu 24.3.2009 14:00
- Tu 31.3.2009 14:00
- Th 2.4.2009 14:00
- Tu 7.4.2009 14:00
- ...

Lecture Topics

- Java and the JVM
- Design flow
  - From VHDL and Java sources to a running system in an FPGA
- VHDL crash course (optional)
- Bytecodes, the instruction set of the JVM
- JOP, the Java Optimized Processor
- Design decisions for JOP
- Real-time and Safety-critical Java
Lab Work

- Intro exercises
  - J OP *Hello World* 10 Points
  - Real-time threads 10 Points
- LEGO robot example 20 Points
  - Small program
  - WCET analysis
- Project 60 Points
Lab Resources

- TI-LAB
  - Hochparterre, room 2
  - Chip cards from Deinhart
  - Upload a Foto
  - 4 PCs with FPGA hardware
  - Whole week access
  - Supervision on Thursdays 14:00-16:00
Projects – a first list

- JVM test cases
- Bytecode instruction frequency, method lengths
  - SPEC jvm98, Kaffe JVM
- NFS (or other network apps) with ejip
- Massive parallel JOP
  - On a big FPGA in am AMD socket (?)
  - DE2-70 board – new memory interface
- java.lang.Thread
- Safety-critical Java on JOP and/or Java SE
- SCJ test cases (TCK for JSR302)
- HW Scheduler (VHDL)
- Your ideas
Tools

- Only free software
  - Java 1.6
  - Quartus web edition
  - Cygwin (gcc, make)
  - ModelSim (free Xilinx or Altera version)
  - (Eclipse)

- Some projects do not require HW
  - HW Simulation with ModelSim
  - JOP SW simulation
Final report

- In the Wiki
- Description of the project
- Problems and solution
- In English
- Short presentation
Next steps

- Further information
  - http://ti.tuwien.ac.at/rts/teaching/courses/jvmhw/

- Enrolment
  - https://ti.tuwien.ac.at/myTI/

- Course start
  - Tuesday 10.3.2008, 14:00
  - Institute Library, Treitlstr. 3/3rd floor