Laborübung Computer Architecture

Introduction

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Goals

- Understanding pipelined design
- Design your own processor
  - Must be pipelined
  - Resolution of pipeline hazards
Outline

- Compare instruction set architectures (ISAs)
- Design your own ISA
  - Reasonably complete (example programs)
- High-level simulation
- Implement your ISA
  - Processor must run in an FPGA
  - Everything else is up to you
  - Performance, size, cost, energy, …
Prerequisites

- Understand how hardware works
  - Registers
  - Combinatorial logic
  - Critical path
  - Parallelism of hardware
- VHDL, Verilog or some other hardware description language
- Hardware Modelling lab course recommended
- Hello World example in Wiki
Organization

- Course takes place at the TILab
  - Treitlstraße 3, Mezzanine, TILab rooms 1 and 2
  - Priority on ti8, ti9 (room 1) and ti18 (room 2)
  - When available: ti10-ti17 (room 2)

- Group work

- Regular meetings
  - Every or every other week
  - Should be attended

- Assignments
Enrollment online http://ti.tuwien.ac.at/myTI

Deadline: Saturday, 9.10.2010

Preferred group members
  - Grouping will be published by 11.10.2010

Upload picture for access card!

Accounts must be picked up by 28.10.2010
  - Remaining accounts will be removed
  - Account pick up on 15.10.2010 after lecture
Assignments

1. Instruction set comparison (10 points)
2. Instruction set design (10)
3. Assembler and simulator (10)
4. Block diagram (10)
5. Simulation I (individual pipeline stages, 5)
6. Simulation II (data hazards, 5)
7. Simulation III (control hazards, 10)
8. Final presentation (20)
Additional Points

- **Feature points**
  - Interrupts: 5 points
  - Program-Download: 5 points
  - External memory: 5 points
  - Special feature X: 5 to 20 points

- **Relative evaluation points**
  - Performance, code size, cost, energy
  - Choose factors (sum = 1, minimum 0.1)
  - Highest weighted result gets 20 points
  - Other designs get points relative to that
Grading Scheme

- S1: 90 - 100 points
- U2: 80 - 89 points
- B3: 65 - 79 points
- G4: 50 - 64 points
- N5: 0 - 49 points

For a positive grade, it is also necessary to present the final hardware.
Dates

Assignment submissions

- 21.10.2010, 14:00: ISA comparison (e-mail)
- 28.10.2010, 14:00: ISA design
- 04.11.2010, 14:00: Asm and simulator
- 11.11.2010, 14:00: Block diagram
- 18.11.2010, 14:00: Simulation I
- 02.10.2010, 14:00: Simulation II
- 16.12.2010, 14:00: Simulation III
- 13.01.2011, 14:00: Preliminary presentation
- 27.01.2011, 14:00: Final presentation
Additional Dates

- None planned yet
- By popular request
- Possible topics
  - Additional lab meetings
  - VHDL refresh
  - Pros and cons of design decisions
First Assignment

- One ISA per group member
- Describe ISA and answer questions
- Translate short C code fragment to assembler
- Compare ISAs
- Details in lab notes
- Due: 21.10.2010
- Hint: ISAs of embedded processors
Focus

- Focus on the processor
- The course is *not* about
  - Writing software tools: command line is sufficient
  - Writing I/O modules: reuse existing modules
- Implement core ISA first
- Multiplication etc. can be added later
Resources

- **Homepage**: [http://ti.tuwien.ac.at/rts/teaching/courses/calu](http://ti.tuwien.ac.at/rts/teaching/courses/calu)
  - Lab notes, slides, leaflet
- **Wiki**: [http://www.soc.tuwien.ac.at/Computer_Architecture_Lab](http://www.soc.tuwien.ac.at/Computer_Architecture_Lab)
- Lecture notes
- Colleagues
Resources II

- David A. Patterson and John L. Hennessy. *Computer Organization and Design: The Hardware/Software Interface*

Design your own processor
  Assignments from initial design to FPGA implementation
Enrollment open until 9.10.2010
  Upload photo for access card!
  Pick up account! After lecture on 15.10.2010
Regular meetings
  Free to work in lab at other times
First assignment due on 21.10.2010
Questions?